DATA CORRECTION USING HAMMING CODING AND HASH FUNCTION AND ITS CUDA IMPLEMENTATION

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Abstract: This article deals with the use of block code for the entire amount of data. A hash function is used to increase the number of errors that can be detected. The automatic parallelization of this code by using special means is considered.

Index Terms: GPGPU, Hamming code, hash function, automatic parallelization.

I. INTRODUCTION

The peculiarity of the block error-correction codes is that they are applied separately to the data blocks. Using graphical accelerator block code can be applied to the entire amount of data as a single unit. It will reduce the number of additional bits to error correcting.

II. MODIFYING THE HAMMING CODE USING A HASH FUNCTION

If we apply the Hamming code [1] to all the data at once, one bit can be corrected with just a few dozen of additional bits. Equality 1 shows how many maximum i-bits of information can be used when applying additional k-bits:

\[
i_{\text{max}} = 2^k - k - 1
\]

For example, 48 additional bits is enough to correct a single error of 281 trillion bits (32 Tbytes).

With the application of (Table 1). It will allow to detect almost any accidental change of data. Given the presence of bitwise instructions in modern processors, it is possible to effectively apply the Hamming code to independent bit positions (Fig. 1). If 1 byte is used as an elementary part of data, then can be corrected up to 8 erroneous bits in different bit positions.

When there are errors in the same bits of different bytes of data, the Hamming code for such bits will not work correctly and may indicate an error in a byte that does not actually have the errors. If we can detect the largest number of errors in a given byte, we can conditionally assume that the Hamming code worked correctly for these bits. This byte can now be considered as a central one and the value of adjacent bytes is matched to the hash function convergence with the expected value. If the assumption was false, it would not be possible to find a value for the hash function convergence, which would indicate an error that cannot be corrected (Fig. 2).

<table>
<thead>
<tr>
<th>Table 1</th>
</tr>
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<tbody>
<tr>
<td><strong>The Hamming code and the hash function</strong></td>
</tr>
<tr>
<td>hash function</td>
</tr>
<tr>
<td>Changes in one bit of data</td>
</tr>
<tr>
<td>Changes in a few bits of data</td>
</tr>
<tr>
<td>Change in a large piece of data</td>
</tr>
<tr>
<td>* Accidentally changing data to obtain the same hash value is unlikely.</td>
</tr>
</tbody>
</table>

![Fig. 1. Multiple Hamming code](image1)

![Fig. 2. Central error byte position](image2)
used, which is the ratio of bits that directly encode data into the total number of code bits. This ratio for effective coding should be close to 1. Fig. 3 shows that this ratio is already approaching 1 for 8 kilobytes of information.

So, the proposed code is based on the following principles:

- all bits in a byte (or 2, 4 or 8 bytes) are encoded independently by the Hamming code;
- all messages are signed by the hash function;
- hash function is repeatedly written and read using the majority function;
- in the case of unsuccessful decoding, when the value of the hash function does not match the message received, an attempt is made to find the central fragment of the error and to select for it and the neighboring fragments of values that would allow to form the correct value of the hash function.

Then the proposed coding (Fig. 4) will contain the hash function and the data represented by the Hamming code. Since the hash value is much smaller, it can be represented by majority coding.

![Fig. 4. Data fields](image)

The total amount of data will be equal to the size of the hash function $5 \times 16$ bytes $= 80$ bytes. The number of additional bits of data for the Hemming code is estimated at 64 bytes. Incremental error codes are used when using codes (Table 2).

In general, there are 5 levels of work with the proposed code (Table 3).

Also, code can be applied in partial modes, and full mode may not look for collisions. In addition, data bits can be used without any functions for error detection and correction, since these bits are presented unchanged. This may be relevant in cases where such code is generated by a stationary computer system and a low-performance embedded computer system acts as the recipient of the data.
Fig. 5 shows a simple algorithm for encoding and error correction when applying the proposed code composition.

III. PARALLELIZATION

Some parts of the proposed algorithm can be parallelized. Firstly, the calculation of the control K-bits of the Hamming code can be parallelized (Fig. 6). Also, hash values (MD5) can be calculated in parallel when selecting values in bytes for various attempts to correct erroneous data.

Fig. 6. Parallel calculation of control bits for the Hamming code

IV. IMPLEMENTATION ON CUDA

From the very beginning of the development of GPGPU technology [3], CUDA technology [2] is mainly used to perform mathematical calculations [4, 5, 6, 7, 8]. Therefore, this technology is well-suited to error-correcting code.

For effective use of CUDA technology, compute process must consist of many execution kernels [9]. Significant restrictions are imposed on the execution of the code of each such kernel [10, 11].

The process of decoding will have the structure which is shown in Fig. 7.

Synchronization points are provided for part of the CUDA code to execute directly on the GPU (Fig. 8).

Each such stream of execution has access to several types of memory (Fig. 9).

The basic code execution constraints on the graphical accelerator will be imposed when working with shared memory [12]. The following macro was created for efficient operation.

![Fig. 8. The model of performance on the graphic accelerator](image)

![Fig. 9. The local context of the workflow for the system](image)
The initialization of the structure of a parallel program is formed as the following function:

```
void cudaRunParallelComputeModel[listing_3]
```

The code for executing such kernels is given in Listing 4.

```
void cudaRunParallelComputeModel[listing_4]
```

In non-hash mode, the CUDA acceleration results are shown in Table 4.

<table>
<thead>
<tr>
<th></th>
<th>Run time for 4MB data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential execution</td>
<td>≈2.192 s</td>
</tr>
<tr>
<td>Run on CUDA</td>
<td>≈0.296 s</td>
</tr>
</tbody>
</table>

In full mode, the CUDA acceleration results are shown in Table 5.

<table>
<thead>
<tr>
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<th>Run time for data size 16kB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential execution</td>
<td>≈19.832 s</td>
</tr>
<tr>
<td>Run on CUDA</td>
<td>≈1.211 s</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The proposed data correction based on Hamming coding and hash function allows:

- to use a small number of additional bits;
- to detect any error;
- to correct errors to attempt to correct multiple errors in adjacent bytes;
- to use 5 different bit positions;
- increased performance when using CUDA technology.

REFERENCES

Anatoliy Melnyk has been a Head of Computer Engineering Department at Lviv Polytechnic National University since 1994. He graduated from Lviv Polytechnic Institute with the Engineer Degree in Computer Engineering in 1978. In 1985 he obtained his Ph.D in Computer Systems at Moscow Power Engineering Institute. In 1992, he received his D.Sc. degree at the Institute of Modelling Problems in Power Engineering of the National Academy of Science of Ukraine. He was recognized for his outstanding contributions into high-performance computer systems design as a Fellow Scientific Researcher in 1988. He became a Professor of Computer Engineering in 1996. From 1982 to 1994 he was a Head of Department of Signal Processing Systems at Lviv Radio Engineering Research Institute. From 1994 to 2008 he was a Scientific Director of the Institute of Measurement and Computer Technique at Lviv Polytechnic National University. From 1999 to 2009 he was a Dean of the Department of Computer and Information Technologies at the Institute of Business and Perspective Technologies, Lviv, Ukraine. Since 2000 he has served as a President and CEO of Intron ltd. He has also been a professor at Kielce University of Technology, University of Information Technology and Management, Rzeszow, University of Bielsko-Biala, John Paul II Catholic University of Lublin.

Nazar Kozak was born in 1985 in Ukraine. He received the B.S. and the M.S. degrees in computer engineering at Lviv Polytechnic National University in 2007 and 2008. He has been doing scientific and research work since 2008. His work resulted in 13 publications. Currently, he is an assistant professor at the Computer Engineering Department, Lviv Polytechnic National University.