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PERSPECTIVE COMPONENTS OF CYBER-PHYSICAL SYSTEMS IMPLEMENTING CONVERSION, CODING DATA EXCHANGE, AND USER COMMUNICATION PROCESSES

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***Abstract*: The methodology of structural organization and microprocessor schematics of perspective components of cyber-physical systems has been described in the article. Such components, according to the concept of a multilayer platform proposed by prof. A. Melnyk, implement processes and integrated technologies of measuring information transformation and generalization of the structure of effective coding, digital processing, data exchange, user communication and decision making.**

Emphasis has been made on providing the utmost minimax, systemic polyfunctional characteristics of these components in structures of cyber-physical systems.

***Index Terms*: Components of Cyber-Physical Systems, Data Exchange Protocols, Information technology, Monitoring of Technological Processes**

I. INTRODUCTION

There are outlined the fundamental concepts of construction and structure of a multilayer platform for cyber-physical systems (CPSs) [1-3]. Basic functions and their applications are formulated. Interaction with the physical world, data gathering, data processing, decision making and personal service are key issues in the development of the theory and principles for implementing this class of multi-layer real-time systems.

Development of CPSs, which provide measurement organization, allow for the calculation, reliable secure transmission, storage, sharing of measurement equipment and service information when influencing physical processes. Particular information and integral compatibility of these components of CPSs allow to increase the level of human interaction with physical systems.

At present, the implementation and concept of building CPSs is particularly relevant in view of the significant advances in the theory of measurement, coding, processing, transmission, use of information data, and the powerful capabilities of micro- and nanotechnologies for the synthesis of computing and communications software.

Significant progress has also been made in the development and implementation of mobile communications with the user and professional operators of computerized remote industrial and biological object monitoring systems.

The author states that modern theoretical substantiation of the principles of control systems construction is insufficient [1, 2]. This is due to the solution of the problem of functional completeness and synergistic effect of components integrating in the system structure. The author also notes that the results of scientific work in the development and application of CPSs demonstrate excellence in the field of integrated, physically integrated computer technologies, intelligent telecommunications tools that provide real-time data collection and feedback information in cyberspace mathematical services, algorithms, computing tools, decision-making methods, and intelligent control of multifunctional data movement.

Particular attention is paid to the functions of CPSs, which must be equipped with high-performance computing facilities and provide effective and reliable information protection in systems of collecting, processing and access to data.

An actual problem in the development of multilayered CPS platforms is the effective use of modern advances and the concept of computer and telecommunications technologies.

A large number of component types of CPSs require the use of high-speed measuring and computing tools that allow them to achieve their required quality of work [4]. It is important to solve the problem of providing users with the necessary information by the technologies of intellectual and expert systems. Improvements to the monitoring components of physical processes and communication tools, including touch screens of audio-video keyboards for technological processes, are relevant in this field. It allows the user to make the right decision. Also, personal service allows to predict user behaviour and user interface interaction with CPSs.

The actual problem is also improving data exchange protocols (DEPs), especially at the basilar level of CPSs.

The development, improvement and research of system components of CPSs with extremely minimal system characteristics are the subjects of research of this article.

There should also be considered the possibility of parallelizing high potential and a substantial increase in performance of computing processes and building information models of monitored object states through the use of problem-oriented special processors, including mobile wireless transmission of data.

II. CRITERIA FOR SYSTEM CHARACTERISTICS OF MICROELECTRONIC COMPONENTS OF CPSS

Estimation of the system characteristics of micro-electronic components of circuit solutions for computing tools are offered in papers [5–6]:

(i)) Hardware costs by Quine based on estimation of the total number of inputs and outputs of the microelectronic structure is calculated according to the expression

$$HC = \sum_{i=1}^{n} X_i + \sum_{j=1}^{m} Y_j , \quad (1)$$

where X_i are inputs, $i \in 1, n$; Y_j are outputs, $j \in 1, m$; n, m are respectively the number of inputs and outputs of the structure.

This estimate is used to calculate the functional complexity of microelectronic devices [6];

(ii) hardware complexity estimation [7, 8] is performed by calculating the number of logic elements and gates in the structure of devices with different number of hierarchies and types of components:

(a) single or different levels – $H_D = \sum_{i=1}^{N} H_i$,

(b) two levels – $H_D = \sum_{\mathrm{j}=1}^{M} \sum_{i=1}^{N} H_{ij}$,

(c) three levels – $H_D = \sum_{\mathrm{j}=1}^{M} \sum_{i=1}^{N} \sum_{\mathrm{k}=1}^{L} H_{ijk}$,

where H_D is overall evaluation of hardware complexity, H_i, H_{ij}, H_{ijk} are evaluation of hardware complexity of each component on different levels, *i, j, k* are types of components or levels of device structure; *M, N, L* are respectively the number of types of different components or levels of structure of the device;

(iii) the time complexity of the structure is calculated by determining the total number of micro-tact delay signals in the longest circuit of sequentially connected logical or functional elements between the respective inputs and outputs of the device:

$$\tau = \sum_{j=1}^{q} \tau_j , \quad (2)$$

where q is the number of connected components in series; τ_j is signal delay in each *j* component;

(iv) estimation of structural complexity [6] of schematic structures, graphic images and polyfunctional data:

$$k_s = \sum_{i=1}^{n} \alpha_i P_i , \quad (2)$$

where $P_i \in (l, P, x, d, r, h, z, b, c, i, n, a, f)$ are informative parameters of structures` attributes, α_i – expert estimates of the complexity coefficient of elements and components of structured data..

The symbols of the attributes of the structural components of the data movement models and expert estimates of the complexity coefficient α_i and the classified informative parameters $l, P, x, d, r, h, z, b, c, i, n, a$ are given in Table 1.

(v) evaluation of structure efficiency [6] is calculated by the relation between information and structural complexity according to the following expression:

$$k_e = K \cdot \frac{F_C}{k_s} \Rightarrow \max , \quad (4)$$

where K is the level identifier; F_C is information complexity of the device.

The mentioned criteria allow to calculate and compare the system characteristics of microelectronic and computing components of cyber-physical systems of the following classes: means of analog-digital, multi-functional coding and digital processing of measurement data, protocols of data exchange between layers of cyber-physical systems, components of special proces-sing systems, means of process monitoring and commu-nication with the operator.

III. HIGH-SPEED DEVICES OF ANALOG-TO-DIGITAL MULTIFUNCTIONAL CODING OF MEASUREMENT DATA

Analog-to-digital converters (ADCs) are one of the basic components of modern microelectronic devices of digital signal processing of cyber-physical systems.

An important and urgent problem is the improvement of structural and schematic solutions of this class of devices according to the system criteria of time, hardware, structural, functional and entropic complexity. Successful solution of the set of problems in the environment of the mentioned problem, taking into account extremely mass duplication and application of parallel type ADC, sets theoretical and scientific-applied problem to synthesize on the basis of CAD their microelectronic circuitry with maximum speed, reduced structural and hardware complexity. Optimization of these ADC characteristics will allow to increase their reliability, reduce dimensions and energy consumption accordingly, which will expand their scope.

In addition, such ADCs are components of more structurally and functionally complex computing tools and special processors of cyber-physical systems. In their synthesis, structural, systemic and functional compatibility with other microelectronic devices must be taken into account.

Table 1

Systematization of expert assessments for structural complexity of graphical structure components

Letter / Value	Symbols	α_i
l / Line		1
		1.5
		1.1
		1.2
		1.2
		1.7
P / Bend		2
		2.2
		2.2
x / Intersection		3
	,	3.1
d / Touching		2
		2.2
r / Branching		4
		6.2
		4.2
h / Method of filling	,	2
	,	2
Z / Directed line		2
		3
		2.4
		2.5
		3.4
		3.5
b / Letter	Aa…Яя, …, *Aa…Яя*, Aa…Яя, …, *Aa…Яя*,	8–10
	Aa…Zz, …, *Aa…Zz* Aa…Zz, …, *Aa…Zz*	8–10
c / Digit	1, 2,…0….	4
i / Index	1, 2,…0, a, A	4
s / Symbol	©, ®, π, ψ, ω, &, %, @, §, Θ, №, ∑, ∫, ∞	4
	☺, ☼ ♫, μ, $, *, €, ∏, ♀, ♂, ♠, ♫…	4
n / Sign	+, -, <, >, =, ±, ≡, ≈..	2
	≠, ≤, ≥, (, “, {, !, ?...	2

Among known classes of ADCs, the maximum speed is provided by ADCs of parallel type [9].

The structure of the advanced ADC [10], which can be effectively used as a high-speed component of processors of cyber-physical systems to convert measurement data into digital form, is shown in Fig. 1.

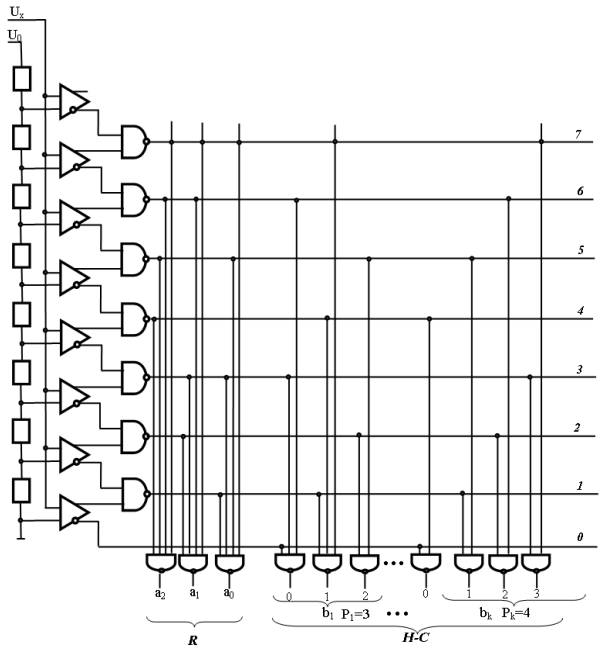

Fig. 1. Structure of the multifunctional parallel ADC with output codes in Rademacher's and Haar-Krestenson's theoretical and numerical basis

The peculiarity of the structure is the simultaneous generation of the output data in the form of binary Rademacher's bases and Haar-Krestenson's residual classes.

The basis for the principle of construction of such ADC is the conversion of the analog signal at the output of the comparator line in the parallel unitary code, the subsequent transformation based on the paraphase outputs of the comparators and the line of logic elements "AND-NOT" in the inverse parallel code of Haar, which is a line of multi-input logic "AND-NOT" simultaneously transforms into a Rademacher's based k-bit binary code and a Haar-Krestenson's parallel code of modular arithmetic of residual classes.

The peculiarity of this structure is the simultaneous generation of the output data in the form of binary Rademacher's bases and Haar-Krestenson's residual classes.

High-speed parallel-based multibasic ADCs based on extended-phase comparators with advanced functionality and source codes on the Rademacher and Haar-Krestenson bases allow to reduce hardware complexity compared to known ADCs (10-bit source code) by 8 times (Haar-Krestenson's source code ($P_1 = 7$, $P_2 = 12$, $P_3 = 13$) and by 14 times (Haar-Krestenson's source code ($P_1 = 32$, $P_2 = 33$). The proposed use of paraphase comparators in the ADC structure allowed to replace structurally complex XOR exclusive elements that contained at least 3÷5 logic elements and 2÷3 sequentially connected logic elements

"AND-NOT", "OR", "And" in each of the 2^k samples of the device, with the logic elements "AND-NOT" with a signal delay by 1ν (v is time delay of the signal in one microelectronic logic gate), which made it possible to reduce the structural complexity and increase its performance, in comparison with analogues, by 2 times with a reduction of the time delay of signals up to 4ν.

That is, this ADC is characterized by a feature of polyfunctionality because it allows computers to perform operations on the digital code by binary arithmetic and modular arithmetic residual classes.

ADCs with Rademacher's baseline binary are characterized by the following functional limitations:

(i) code redundancy, since ranges of measurement parameters change for standard accuracy classes of sensors are given in decimal number system (1.0; 0.5; 0.1; 0.025), and ADCs with source binary codes, respectively, in the range of 2^k where k is the digit of ADC (k = 7, 8, 10, 12);

(ii) speed of binary code calculation of the following type: addition $(x_i - y_i)$, squaring (x_i^2), multiplication $(x_i \cdot y_i)$, determination of modular $(|x_i - y_i|)$ and quadratic difference $(x_i - y_i)^2$ of estimates of Euclidean distance, accumulation of digital sum of values $(\sum_{i=1}^{n} x_i)$, modular differences $(\sum_{i=1}^{n} |x_i - y_i|)$, sum of squares of differences $(\sum_{i=1}^{n} (x_i - y_i)^2)$, etc. in binary arithmetic codes by an $1 \div 3$ order of magnitude lower than the speed of similar calculations in Haar-Krestenson's codes according to modular arithmetic of residue classes. [5,11-13].

Such an increase in the speed of calculations in the residue classes is due to the lack of end-to-end transfers when performing arithmetic operations on the residues. The representation of measurement information in CPSs in Haar-Krestenson's residual codes, regardless of the accuracy of the calculations, equals to ones of micro clock signals. The efficiency of the representation and digital processing of measurement information in the Haar-Krestenson's codes is confirmed by the successful development of special processors of analog-to-digital conversion and the implementation of computational processes in adders, multipliers, correlators and spectral analysers.

Thus, the development of systems of simple modules for the implementation of high-speed computations of measurement information in cyber-physical systems is an urgent application problem, which provides opportunities to significantly improve the speed of software and special processing computing in the field of computerized measuring technology.

The system parameter of this method of encoding and processing the measurement data is a nearly 2÷3-fold increase in the bit rate of the Haar-Krestenson's codes compared to the Rademacher's binary codes. At the same time, the high level of modern microelectronic technology is a positive factor in simplifying the processes of designing and microelectronic implementation of software and hardware components of cyber-physical systems.

Calculation of the module systems of analog-digital encoder with Haar-Krestenson's source codes conditioned to accuracy classes of sensors of information-measuring CPSs is as follows:

1.0 $0 \le x_i \le 100$;
0.5 $0 \le x_i \le 200$;
0.1 $0 \le x_i \le 1000$;
0.05 $0 \le x_i \le 2000$;
0.025 $0 \le x_i \le 4000$;
0.000015 $0 \le x_i \le 65536$.

Sets of relatively simple modules for such sensor accuracy classes are presented in Table 2.

Table 2

Sets of relatively simple modules

Range x_i	P_1	P_2	P_3	P_4	P_0
100	4	25	–	–	100
	3	5	7	–	105
	2	3	17	–	102
	10	11	–	–	110
	9	13			117
	8	13			104
200	2	3	5	7	210
	3	4	17		204
	4	5	11		220
	13	16			208
1000	31	33			1023
	5	11	19		1045
	2	3	7	25	1000
	6	7	25		1000
	7	8	19		1064
2000	2	31	33		2046
	10	11	19		2090
	3	4	7	25	2000
	7	12	25		2000
4000	4	31	33		4092
	11	19	20		4180
	4	5	11	19	4180
	16	15	17		4080

Let us consider some examples of solving some problems of processing RGB pixels of optical images based on the presentation of measurement information in Haar-Krestenson's (H-K) codes.

The color coding of pixels in the Hamming space of the monitor given in Cartesian coordinates can be uniquely represented in the residual classes system (RCS) of Krestenson's theoretical numerical basis (TNB). This representation is implemented by specifying three relatively simple modules (P_1, P_2, P_3), that allow one pixel of RGB system to be uniquely encoded in the binary system of Rademacher TNB calculation by

performing a direct integer transformation of the RCS according to the expression [14]:

$$N_k = res \sum_{i=1}^{3} b_i \cdot B_i (\text{mod } P_0), \quad (5)$$

where b_i is a smallest integral residue, B_i are orthogonal RCS bases calculated according to the Diophantine equations:

$$\begin{aligned} B_1 &= P_2 \cdot P_3 \cdot m_1 \equiv 1(\text{mod } P_1); \\ B_2 &= P_1 \cdot P_3 \cdot m_2 \equiv 1(\text{mod } P_2); \\ B_3 &= P_1 \cdot P_2 \cdot m_3 \equiv 1(\text{mod } P_3), \end{aligned} \quad (6)$$

where m_1, m_2, m_3 are inverted elements of the RCS code, $P_0=P_1 \cdot P_2 \cdot P_3$ is the pixel color coding range of the bitmap $K_0 = \hat{E}[\log_2 P_0]$, $\hat{E}$ is an integer function with rounding to a larger integer.

Unambiguous RGB-pixel encoding in the Rademacher-Krestenson's basis is ensured by selecting the following values of the residual encoding range bi in the Rademacher's basis:

$b_1 = b_R; 0 \le b_R \le 255; (00000000 \div 11111111);$

$b_2 = b_G; 0 \le b_G \le 254;$

$(00000000 \div 11111111);$

$b_3 = b_B; 0 \le b_B \le 255; (00000000 \div 11111111);$

In addition, given the coefficients $m = 1.0$, $n = 4.5907$, $p = 0.0601$, for the most saturated green color, the range of its change can be specified in the range of $0 \le b_G \le 254$, which allows to ensure the mutual simplicity of the modules, P_1 =256,– P_2 = = 255– P_3 =257.

To check the mutual simplicity of the selected system of modules, we decompose them into the following factors: $256=2^8$, $255=5 \cdot 51$, 257 is a prime number, that is P_0=1677690, where P_0<16777216. Therefore, the condition of formation of 24-bit pixel code in the Rademacher-Krestenson's basis is satisfied.

In a Rademacher's binary system, the module codes have the following representation:

$P_1=100000000_{(2)}$; $P_2=11111111_{(2)}$;

$P_3=100000001_{(2)}$;

Then

$P_0=111111111111111100000001_{(2)}$.

Since there is a module $P_1=2^8$ among the $P_1 \cdot P_2 \cdot P_3$ modules, the remainder of the number N_k (G is the color sign), according to the inverse transformation of the RCS, will be represented without decoding by 8 lower bits of the number represented in the Rademacher's basis.

According to the solution of the Diophantine equations (6), we obtain the following values of inverted m_i elements and basis numbers B_i:

m_1=255; B_1=16711425; m_2=128; B_2=8421376;

m_3=129; B_1=8421120.

Make sure that you have actually implemented the UCC transition data that was used by level:

$$N_k = (b_R \cdot B_1 + b_G \cdot B_2 + b_B \cdot B_3) \cdot (\text{mod } P_0) = 1,$$

where b_R=1, b_G=1, b_B=1

thus,

N_k=(1·16711425+1·8421376+1·8421120) modP_0=1.

E.g.

N_k=(10·16711425+200·8421376+100·8421120)– –(mod 6776960) =9187850,

corresponding to the binary representation of the RGB pixel at the Krestenson's basis

$(100011000011001000001010_2)$.

The decoding of such an RGB pixel representation is as follows:

r_i=res N_k(modP_1); g_i=res N_k(modP_2);

b_i=res N_k(modP_3).

RGB color pixel encoding is performed by a 24-bit binary code, where the intensities of each color are represented by 8-bit Rademacher's binary codes [15]:

$$R\begin{cases} r_{8-1} \\ \dots \\ r_i \\ \dots \\ r_0 \end{cases} \quad G\begin{cases} g_{8-1} \\ \dots \\ g_i \\ \dots \\ g_0 \end{cases} \quad B\begin{cases} b_{8-1} \\ \dots \\ b_i \\ \dots \\ b_0 \end{cases} \quad (7)$$

$$0 \le r_i \le 255 \quad 0 \le g_i \le 255 \quad 0 \le b_i \le 255$$

We encode RGB pixels of color images in the Rademacher-Krestenson's and Haar-Krestenson's TNBs by selecting a system of relatively simple modules (P_1, P_2, P_3) whose product exceeds the quantization range of brightness values (r_i, g_i, b_i). This condition may be satisfied by a different set of discrete RCS conversion modules, such as: (P_1=5, P_2=7, P_3=8) which provides unambiguous brightness encoding r_i, g_i, and b_i and range P_0=5·7·8=280>255. The following is a code structure in the R-K's basis, which uniquely represents the corresponding RGB-pixel code:

$$R \vee G \vee B\begin{cases} a_2 \\ a_1; \\ a_0 \end{cases} \quad R\begin{cases} c_2 \\ c_1; \\ c_0 \end{cases} \quad \begin{cases} d_2 \\ d_1; \\ d_0 \end{cases}$$

$$P_1 = 5 \qquad P_2 = 7 \qquad P_3 = 8 \quad (8)$$

where $a_i \in \overline{0,1}$; $c_i \in \overline{0,1}$; $d_i \in \overline{0,1}$ $i_i \in \overline{0,2}$.

The scheme of representation of RGB-pixel in the vector space of the system of residual classes is shown in Fig. 2.

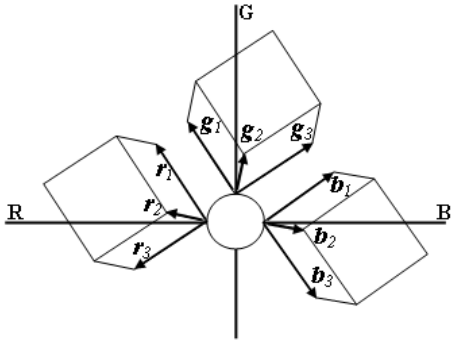

Fig. 2. Representation of RGB-pixel in the vector space of the system of residual classes

Each value a_i, c_i, d_i is calculated as a residue according to the following expressions a_i=res (r_i modP_1); c_i=res (g_i modP_2), d_i=res (b_i modP_3).

For a given set of modules, we calculate the inverted elements m_i and basis numbers B_i according to the solutions of the Diophantine equations (6), and we obtain:

m_1=1; B_1=56; m_2=3; B_2=120; m_3=3; B_1=105.

We check the values m_i and B_i according to expression as follows (4):

N_1=(1·56+1·120+1·105)(mod 280)=1.

Consider the example. Let the RGB pixel color intensities be set as r_i=10, g_i=100, b_i=37 .

Then we get the RGB pixel codes in the bases of:

1). Rademacher's: r_i=00001010$_{(2)}$, g_i=01100100$_{(2)}$, b_i=00100101$_{(2)}$.

2) Rademacher-Krestenson's:

$$r_i = (\overbrace{000}^{P_1}\overbrace{011}^{P_2}\overbrace{101}^{P_3})_{(5,7,8)};\ g_i = (\overbrace{000}^{P_1}\overbrace{010}^{P_2}\overbrace{010}^{P_3})_{(5,7,8)};$$

$$b_i = (\overbrace{010}^{P_1}\overbrace{010}^{P_2}\overbrace{101}^{P_3})_{(5,7,8)}.$$

The representation of the RGB-pixel code in the Haar-Krestenson basis for each intensity value r_i, g_i, and b_i is performed according to the following structure:

$$R \vee G \vee B \begin{cases} a_{P_1-1} \\ .... \\ a_i \\ .... \\ a_0 \end{cases}; \quad \begin{cases} c_{P_2-1} \\ ... \\ c_i \\ ... \\ c_0 \end{cases}; \quad \begin{cases} d_{P_3-1} \\ ... \\ d_i \\ ... \\ d_0 \end{cases}; \quad (9)$$

$$P_1 = 5 \qquad P_2 = 7 \qquad P_3 = 8$$

where $i \in \overline{0, P_i - 1}$.

For such RGB pixel color intensity settings as r_i =10 g_i=100 and b_i=37 we obtain the corresponding code structure in the H-C basis

r_i=(10000..0001000..00100000);

g_i=(10000..0010000..00100000);

b_i=(00100..0010000..00000100);

Representation of digital values of color brightness r_i, g_i, and b_i in different TNBs, respectively, causes different bit structures of codes according to the following expressions:

1. On the basis of Rademacher's (R):

$$K_R = \log_2 2^8 = 8 \ \ bits \ .$$

2. On the basis of Rademacher-Krestenson's (R-K):

$$K_{R-K} = \sum_{i-1}^{3} [\hat{E}(\log_2 P_i - 1)] = 3 + 3 + 3 = 9 \ \ bits \cdot$$

3. On the basis of Haar-Krestenson's (H-K):

$$K_{H-K} = \sum_{i=1}^{n} P_i = 5 + 7 + 8 = 20 \ \ bits \cdot$$

IV. EFFECTIVE CODING OF MEASUREMENT INFORMATION AND IMPROVEMENT OF DATA EXCHANGE PROTOCOLS

Research of the system characteristics of such a class of spatially distributed time monitoring systems demonstrates a number of their functional constraints and structural disadvantages [15, 16]:

i) the use of a single ADC with 16- and 24-bit digit is superfluous for a wide class of technological processes in many industries, the objects of which are equipped with sensors of precision classes 0.05÷0.5. Table and trend display of measurement data are not accurately available for quality and real-time analysis by operators of industrial installations.

ii) if the accuracy class of the sensors does not exceed the bit, the digital processing of the measurement data in the range of bits will be significantly distorted by noise and error with the amplitudes of bits.

iii) standard data exchange protocols (DEPs) are used in computer networks (CN) such as Ethernet, Token Ring, FDDI, PPP, Frame Relay, HDLC [17].

The systematization of the channel and physical level structures of the CN frames is carried out in the article and is given in Table 3. Here, the following denotations are used: PA (Preamble), SD (Start Delimiter), FC (Frame Control), DA (Destination Address), AC (Access Control), SA (Source Address), PDU (Packet Data Unit), FCS (Frame Check Sequence), CRC (Cyclic Redundancy Check), ED/FS (End Delimiter/Frame Status), FT (Frame Type), and F (Flag).

Table 3

The structure of the channel and physical layer of CN protocol frameworks

Protocol	Frame Structure (Bits)																			
Ethernet	**PA**		**SD**		**DA**		**SA**		**FT**		**PDU**								**FCS**	
	56		8		48		48		16		512-32K								32	
Token Ring			**SD**	**AC**	**FC**	**DA**	**SA**	**PDU**									**CRC**	**ED**	**FS**	
			8	8	8	48	48	up to 18,2Kx8									32	8	8	
FDDI			**PA**	**SD**	**FC**	**DA**	**SA**	**PDU**									**FCS**	**ED/FS**		
			16	8	8	48	48	up to 4478x8									32	16		
HDLC	**F**	**Address**		**FC**		**Information**										**FCS**			**F**	
	8	8		8 or 16		Variable length, 0 or more x8										16 or 32			8	
PPP	**F**	**Address**	**FC**	**Protocol**		**Information**										**FCS**			**F**	
	8	8	8	8 or 16		Variable length, 0 or more x8										16 or 32			8	
Frame Relay			**F**	**Address**		**Information**										**FCS**	**F**			
			8	8 -16		Variable length,										16	8			

The feature of the frame of the most common HDLC protocol [17] is the possibility of a code combination of the flag (01111110) in the middle of its structure, which leads to crashes and incorrect frame synchronization. The use of the bit-staging operation, which implements an insert "0" after every five odd bits in the structure of the frame, solves this problem by removing such inserts by the processor on the receiving side of the communication channel. Such a structured organization of the HDLC frame leads to random changes in the length of data packets, which become a source of additional errors that may occur when inserting and erasing bits due to interference in communication channels.

Therefore, an urgent problem is the improvement of the methods of encoding the flow of measurement data, provided that their redundancy is reduced by teleportation and systematic coordination with the requirements of structural organization and synchronization of data exchange protocols.

A promising approach to solving this problem is the effective application of the theory of structuring multifunctional data, as well as the improvement of methods for constructing informational neuro models of the operator as a subject of law [17, 18].

According to the theoretical bases and methodology of measurement organization at the basilar levels of computerized distribution systems for monitoring technological processes [19], amplitude ranges of sensor analog signals are internationally standardized. The redundancy bands that occur when binary coding of standard signal changes ranges at sensor outputs of a certain accuracy class is shown in Table 4.

It is known that amplitudes of analog signal sensors are standardized in ranges [19]: 0÷5 mA, 5÷20 mA, 0÷1V, 1÷10V, 0÷2 kHz etc.

There are used ADCs with a digit of (7-8, 8-12, 12-16, 16-24) bits for the following ranges of changes in the amplitudes of sensor signals (1; 2; 5; 10; 20) V in industry. The main companies – manufacturers of ADC are Texas Instruments, Analog Devices etc.

Table 4

The ranges of binary code redundancy in line with the classes of accuracy

Accuracy Class of Sensors	Amplitude of Analog Signals	Binary Code Boundaries on ADC Outputs	Digits of ADC Codes (Bits)	Range of Redundant Binary Codes
1.0	0÷100	0÷128	7	101÷127
0.5	0÷200	0÷256	8	201÷255
0.2	0÷500	0÷512	9	501÷511
0.1	0÷1000	0÷1024	10	1001÷1023
0.05	0÷2000	0÷2048	11	2001÷2047
0.025	0÷4000	0÷4096	12	4001÷4095
0.001	0÷65000	0÷65536	16	65001÷65535

The analysis of Table 2 shows that digital 7-bit measurement data in the range of units are represented by binary codes in the range of (0000000÷1100011), and the codes (1100111÷1111111) are redundant and can be applied as register and service codes in the data exchange protocols.

It is shown the boundaries of informational and redundant binary codes change in accordance with the accuracy class of sensors in Table 5.

There are examples of register pairs of odd and even 7-bit register and service codes R_i. in Tables 6 and 7.

Table 5

The boundaries of informational and redundant binary code changes in accordance with the accuracy class of sensors

Accuracy Class of Sensors	Amplitude of Analog Signals	Informational Binary Code Boundaries	Boundaries of Redundant Binary Codes
1.0	0÷100	0000000 ÷ 1100011	1100111 ÷ 1111111
0.5	0÷200	00000000 ÷ 11000111	11001001 ÷ 11111111
0.025	0÷4000	0000000000 ÷ 1111100111	111110100001 ÷ 111111111111

Table 6

Odd registry codes

Bits	Transmission Codes	Register Code of Protocol Frames						
	0÷99	103	107	111	115	119	123	127
a_6	0 1	1	1	1	1	1	1	1
a_5	0 1	1	1	1	1	1	1	1
a_4	0 0	0	0	0	1	1	1	1
a_3	0 … 0	0	1	1	0	0	1	1
a_2	0 0	1	0	1	0	1	0	1
a_1	0 1	1	1	1	1	1	1	1
a_0	0 1	1	1	1	1	1	1	1

Table 7

Even registry codes

Bits	Transmission Codes	Register Code of Protocol Frames						
	0÷99	100	102	104	106	108	110	126
a_6	0 1	1	1	1	1	1	1	1
a_5	0 1	1	1	1	1	1	1	1
a_4	0 0	0	0	0	0	0	0	1
a_3	0 … 0	0	1	0	1	1	1	1
a_2	0 0	1	0	1	0	1	1	1
a_1	0 1	0	1	1	1	0	1	1
a_0	0 1	0	1	0	0	0	0	0

There are examples of register pairs of odd 8-bit register and service codes Ri in Table 8.

There are examples of HDLC frame protocol formation based on the use of investigated redundant binary codes in the form of flag codes and register codes of structural components of this protocol with 7, 8, 6,

and 4-bit digits of frames. PDU (Packet Data Unit) in Tables 9, 10, 11, and 12.

When encoding data according to the proposed information technology, it is necessary to take into account the bit-oriented digit in the components of the frame structure A1, A2, Y, CRC, as well as the relevant alphanumeric data tables, according to the international ASCII standard, with the size of the registers, oriented on the ranges 0÷99, 0÷199, 0÷999 and 0÷3999. For example, in the digit the addresses of subscribers A1, A2 32 bits in the structure of the protocols (Table 8–11) correspondingly, there must be met the following conditions in the protocols:

– 3·4 bit 9·6=54 bit.

– 2·6 bit 6·6=36 bit;

– 7 bit 7·5=35 bit;

– 8 bit 8·5=40 bit;

Table 8

Even registry codes

Bits	Transmiss-ion Codes	Register Code of Protocol Frames						
	0÷99	201	205	209	213	217	221	225
a_7	0 1	1	1	1	1	1	1	1
a_6	0 1	1	1	1	1	1	1	1
a_5	0 0	0	0	0	0	0	0	1
a_4	0 … 0	0	0	1	1	1	1	0
a_3	0 0	1	1	0	0	1	1	0
a_2	0 1	0	1	0	1	0	1	0
a_1	0 1	1	0	0	0	0	0	0
a_0	0 1	1	1	1	1	1	1	1
	0÷99	229	233	237	241	245	249	253
a_7	0 1	1	1	1	1	1	1	1
a_6	0 1	1	1	1	1	1	1	1
a_5	0 0	1	1	1	1	1	1	1
a_4	0 … 0	0	0	0	1	1	1	1
a_3	0 0	0	1	1	0	0	1	1
a_2	0 1	1	0	1	0	1	0	1
a_1	0 1	0	0	0	0	0	0	0
a_0	0 1	1	1	1	1	1	1	1

Table 8

The structure of 4-bit protocol frame HDLC

Flag	R1	A1	R2	A2	R3
1 1 0	1 1 0		1 1 0		1 1 0
1 0 0	1 0 0		1 0 0	„ „	1 0 0
1 1 0	1 1 0	…	1 1 1	…	1 1 1
1 0 0	1 1 1		1 1 0		1 1 1
Y	R4	PDU	R5	CRC	Flag
.	1 1 0	. . .	1 1 1	.	1 1 1
.	1 0 1	. . .	1 1 1	.	1 0 1
.	1 1 0	. . .	1 0 1	.	1 1 1
	1 1 0		1 1 1		1 1 0

Table 9

The structure of 6-bit protocol frame HDLC

Flag	R1	A1	R2	A2	R3
1 1	1 1		1 0		1 0
1 1	1 1		1 1		1 1
1 1	1 1		1 1	„ „	1 1
1 1	1 1	…	1 1	…	1 1
1 1	1 1		1 1		1 0
0 0	0 1		1 0		1 1
Y	R4	PDU	R5	CRC	Flag
	1 0		1 0		1 1
.	1 1	. . .	1 1	.	1 1
.	1 1	. . .	1 0	.	1 1
.	1 0	. . .	1 1	.	1 1
	1 1		1 1		1 1
	1 1		1 1		0 0

Table 10

The structure of 7-bit protocol frame HDLC

Flag	R1	A1	R2	A2	R3
1 1	1		1		1
1 1	1		1		1
1 1	0		0		0
1 1	0	…	1	…	1
1 1	1		0		1
1 1	1		1		1
0 0	1		1		1
Y	R4	PDU	R5	CRC	Flag
	1		1		1 1
	1		1		1 1
.	1	. . .	1	.	1 1
.	0	. . .	0	.	1 1
.	0	. . .	1	.	1 1
	1		0		1 1
	1		0		0 0

Table 11

The structure of 8-bit protocol frame HDLC

Flag	R1	A1	R2	A2	R3
1 0	1		1		1
1 1	1		1		1
1 1	0		0		0
1 1	0		1		1
1 1	1	…	0	…	1
1 1	1		1		1
1 1	1		1		1
1 0	1		1		1
Y	R4	PDU	R5	CRC	Flag
	1		1		1 0
	1		1		1 1
	1		1		1 1
.	0	. . .	1	.	1 1
.	0	. . .	0	.	1 1
.	1	. . .	1	.	1 1
	1		1		1 1
	1		1		1 0

The appropriate ensuring of the required digit of other components in the proposed protocols should be implemented in a similar way.

It is obvious that some of the most effective structures of data exchange protocols based on the proposed informational technology can be protected by relevant national or international standards.

The advantage of such data exchange frame protocols structuring and coding method is equivalent to the HDLC frame structure, the lack of implementation of "bit stuffing" operation. Such solution liquidates accidental variations of the number of bits in data units that are transmitted in the CN.

To provide increased reliability of staff frame synchronization, flags are supplemented by idle bytes (11111111). That is, the DEP's frame receives the structure as it is shown in Fig. 3.

← Direction of Transmission

	SD	PDU	ED	
11111111	01111110		01111110	11111111

Fig. 3. Structure of the DEP's frame with the enhanced synchronization reliability

The frame structure of the MAC 802.3 protocol is shown in Fig. 4.

← 46-1500 →

PA	SFD	DA	SA	L	LLC	PH	FCS
7	1	6	6	2	≥0	≥0	4

Fig. 4. The frame structure of the MAC 802.3 protocol (Bytes)

This protocol contains the Start Frame Delimiter (SFD) – 10101011 after the preamble (PA). Logical Link Control (LLC) Layer contains two bytes – Length (L) that defines the maximum length of a frame of 1518 bytes without a preamble and a limiter – Placeholder (PH). The filler in the frame structure contains bytes that are added to ensure collision detection. Frame Check Sequence (FCS) contains a 32-bit cyclic code with a convolution without a preamble, a limiter and the control code itself.

The parity check is implemented in the symbols of the IRA alphabet where a parity bit is added to the 7-bit IRA character code.

A known frame synchronization method is implemented by putting into the data stream a special marker in the form of a single bit or a code word with special correlation properties. For example, such properties are one-dimensional and two-dimensional Barker codes and Willard codes.

At the physical level of basilar and local CN, using Manchester's signal manipulation method, frontal frame synchronization is used as start-up triggers in the form of "failures" of Manchester Codes (Fig. 5).

There is also a Deferential Manchester code with a corresponding start-stop implementation of frames (Fig. 6).

Expanded baseband Haar basis for frame synchronization is used in HP-IL protocol (Fig. 7).

PA	SD	PDU	ED
	JK0JK000		JK1JK111

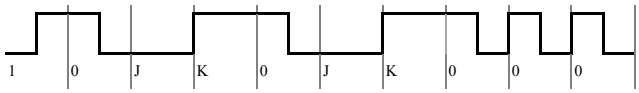

Fig. 5. Start triggers formation for DEPs based on the Manchester FM code

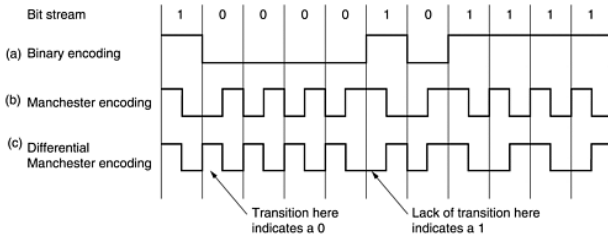

Fig.6 (a) Binary encoding. (b) Manchester encoding. (c) Differential Manchester encoding

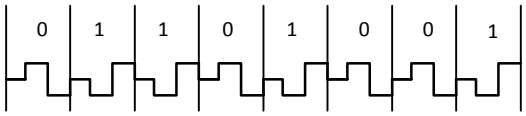

Fig. 7. Forming of HP- IL frame synchronization signals

The using of 2^k+1 signal in systems with amplitude, phase and frequency manipulation proposed in papers [17,20] allowed to substantially simplify the solution of the problem of personnel and bit synchronization in the DEPs. The basic principle of such synchronization is the non-repetition of two identical signs of manipulation in the frame structure and any of them in the secondary one at the frames. Examples of implementation of such start-stop protocol frames synchronization principle are shown in Fig. 8 [20].

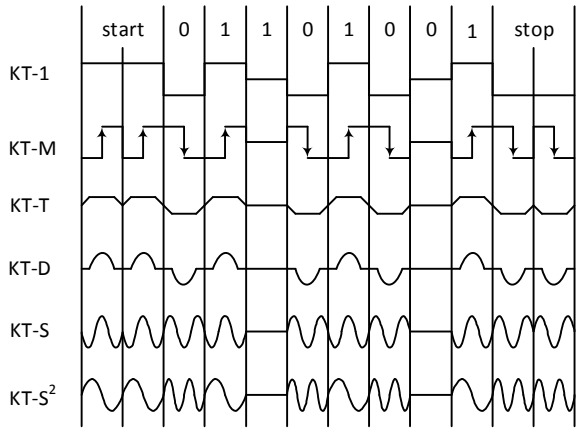

Fig. 8. Synchronization of frames for ensembles of manipulated signals (2^k +1) – ary spaces

A method of manipulating frequency signals with a minimum shift keying (MSK) has received widespread use in the CN. This method is the development of

continuous phase modulation (CPM) technology suggested by S. Pasupathy, it is a partial case of continuous-phase frequency-shift keying (CPFSK), or as a partial case of offset quadrature phase-shift keying (OQPSK) with sinusoidal signal weighing (Fig. 9).

Data transfer rate by QPSK is two times faster as compared to MSK. There are no phase transition frequencies of 180° and the envelope of OQPSK therefore, after non-linear transfer of inheritance, the basic eliminated and high-quality components of such manipulation signals are not amplified.

The disadvantage of the MSK method is the lack of bit and block synchronization of the DEPs frames, as well as the detection and correction of errors in the process of transmitting signals at the CN physical level. The improvement of MSK technology was proposed by manipulating the bi-directional data flow by a recurrent sequence of Galois bits [20].

An example of such technology for manipulating signals with expanded functionality when applying the same number and type of phase-frequency signals (GMSK) is shown in Fig. 10. The essence of the proposed technology is that the bits of units in the data packet are numbered by the recurrent Galois code G^2_k. Moreover, for units in the data packet, the Galois bit "1" is transmitted by the frequency MSK (f_{11}), and the Galois bit "0" is transmitted at the MSK frequency (f_{12}). The difference between frequencies is half the speed of data transmission. The bits of zeros in the data packet are also numbered by the recurrent Galois code G^2_k. Moreover, for zeros in the data packet, the Galois bit is "1" at the MSK frequency (f_{21}), and the Galois bit "0" is transmitted by the frequency MSK (f_{22}).

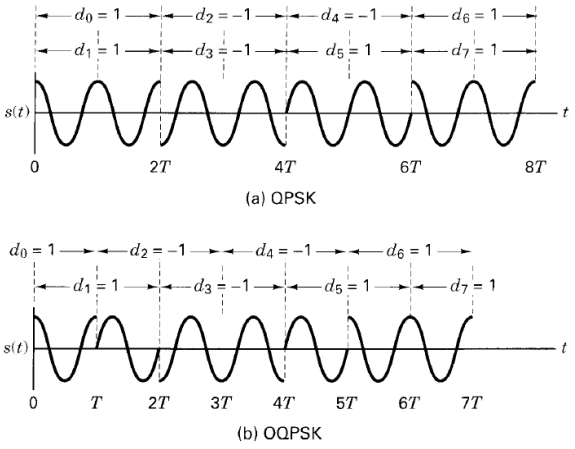

Fig. 9. QPSK (a) and OQPSK waveforms (b)

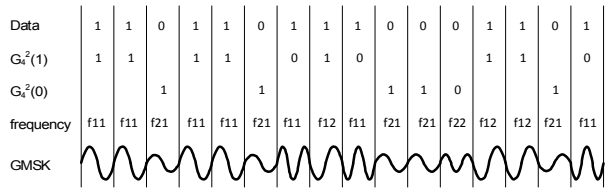

Fig. 10. Technology of manipulating the phase-frequency signal based on the Galois codes

The difference between frequencies is half the speed of data transmission. The frequencies (f_{11} and f_{12}) used to transmit the packet "1" differ in frequency amplitude (f_{21} and f_{22}), which are used to transmit the packet "0". The application of the Galois code in MSK technology greatly extends the functionality of the frame structure of the DEPs, which provides a reliable block and bit frame synchronization, as well as the ability to detect and correct single and multiple errors in the process of receiving manipulated signals at the CN physical level.

Furthermore, reducing the digit of the protocol frames allows to use assembly with less amount of manipulated signals, and this fact increases interference resistance of the teleportation data in the communication channels. It also multifunctionally simplifies the teleportation problem without additional transformations of 4-bit alphanumeric data codes that are formed by two 4-bit codes at the output of synthesized key frames. Modern software tools make it easy to ensure the compatibility of the proposed protocol structures with existing standard protocols in computer networks by transforming their structures. More reliable detection and identification of deviations of object states from normalcy at the lower levels of spatially distributed information and measurement systems under the intense industrial interference is achieved by more strict structuring of the frames components, accompanied by register codes

V. SUPER HIGH-SPEED CONVERTERS AND PROCESSORS IN THE HAAR-KRESTENSON'S BASIS CODES

According to the squared Euclidean distance, it is necessary to use the operation of squaring the modular difference codes of analog signals, which requires the use of matrix multipliers and leads to a significant decrease in the speed, an increase of hardware and structural complexity of this processor class in the Rademacher's basis. Therefore, there is proposed a block diagram of a difference-modular squarer [21], which is a component of the Hemming distance determination device and is implemented in the codes of Haar-Krestenson's basis.

This difference-module squarer is used as a high-speed component in solving problems of statistical analysis and implementation of high-performance components of special processors for determining the Hemming distance according to the squared Euclidean distance estimation $Z = (x_i - y_i)^2$.

The structure of the high-performance special processor, proposed by the author, contains 2 parallel-type ADCs with source codes of Haar-Krestenson's basis, implemented by the use of modular arithmetic of residual classes system (RCS) and Haar-Krestenson's code matrixes (Fig. 11) [21].

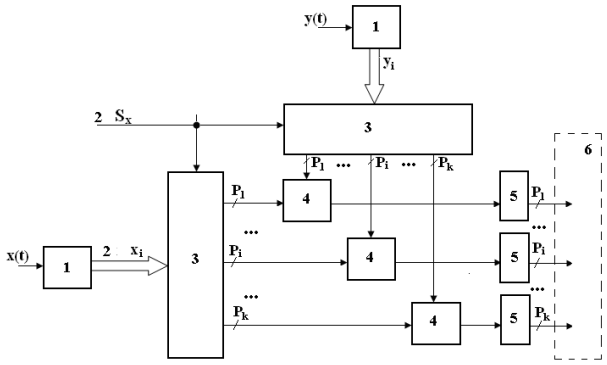

Fig. 11. Structural diagram of the difference-modular squarer

The device (Fig. 11) contains: ADC of parallel type (1) with the corresponding Haar-Krestenson's source codes x_i and y_i (x_i=(a_1, a_2,…,a_i,…,a_k), y_i=(b_1, b_2,…,b_i, …,b_k), a_i=res x_i(modP_i), b_i=res y_i(modP_i)) $i \in \overline{1,k}$, k is the number of modules of the Haar-Krestenson's codes), the synchronization bus S_x(2) that generates the recording signals of codes x_i and y_i in the register memory on the D-triggers (3), the matrix of determining the modular differences for each P_i module (4), the modular squares in Haar-Krestenson's basis (5), output bus (6).

The implementation and structure example of the input and output connection of the difference-module matrix on the logical elements "AND-NOT" (P=11) is shown in Fig. 12.

The structural implementation of the code formation of the square modular difference $((a_i-b_i)^2 \text{mod} P_i)$ in the Haar-Krestenson's basis on the logical elements "AND-NOT" (P=11) is shown in Fig. 13.

According to the properties of the residual classes number system for the unique representation of the square of the difference of the two numbers $(x_i-y_i)^2$, there must be fulfilled the following condition: the product P_0 of mutually simple modules P_i must be equal or greater than N=[(x_i-y_i)max], which corresponds to the condition: the sum of the binary bits of the modules P_i must be 1–2 bits larger relative to the number of bits of the binary representation of the difference between the numbers x_i and y_i, i.e.: $n \geq \hat{E}[\log_2 N^2]$, where $\hat{E}$ is an integer function with rounding to a larger integer. E.g. for the number of modules P_i, k=4 and the maximum values of squares N. The calculations for the various N are shown in Table 12

The peculiarity of the device (Fig. 11) is the independence of the formation of a direct square code at the outputs of the modules of the squares (5), regardless of whether the direct or inverted module codes are formed at the outputs of the difference-modular matrices (4).

E.g., we need to define the square of the difference between two numbers that can be represented in the range: $0 \leq x_i \leq 127$, $0 \leq y_i \leq 127$ the maximum value of the square of their differences is equal to 127^2=16129.

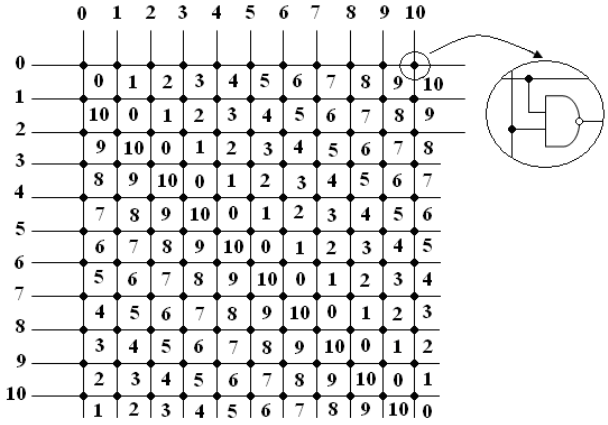

Fig. 12. The difference-modular matrix on the elements of "AND-NOT"

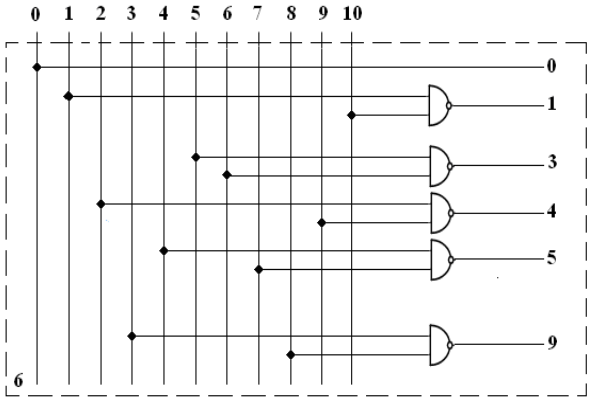

Fig. 13. Implementation of the formation of a modular difference square code $((a_i-b_i)^2 \text{mod} P_i)$ in the Haar-Krestenson's basis

Table 12

Example of maximum square values

		P_1	P_2	P_3	P_4	n	N^2	P_0
N	15	2	3	5	11	9	225	330
n	4	1	2	3	4			
N	99	8	9	11	13	15	9801	10296
n	7	3	4	4	4			
N	255	13	16	17	19	18	65025	67194
n	8	4	4	5	5			
N	1023	29	32	33	37	22	1046529	1133088
n	10	5	5	6	6			
N	2047	43	45	47	49	24	4190209	4456305
n	12	6	6	6	6			

Let us represent the given numbers x_i=29, y_i=17 in Rademacher-Krestenson's (R-K) and Haar-Krestenson's (H-K) basis in the residual classes number system with a set of modules: P_1=8, P_2=9, P_3=11, P_4=13, the product of which is equal to 8–9–11–13=10296>9801, i.e. in the R-K's codes x_i=$29_{(10)}$= $(5\ 2\ 7\ 3)_{(8,9,11,13)}$, y_i=$17_{(10)}$= $(1\ 8\ 6\ 4)_{(8,9,11,13)}$, we will subtract these numbers in two variants in the residual classes system and square the obtained differences:

P_i	8	9	11	13	…	P_i	8	9	11	13	…
x_i	5	2	7	3		x_i	1	8	6	4	
y_i	1	8	6	4		y_i	5	2	7	3	
(x_i-y_i)	4	3	1	12		(x_i-y_i)	4	6	10	1	
	4	3	1	12			4	6	10	1	
$(x_i-y_i)^2$	0	0	1	1	=	$(x_i-y_i)^2$	0	0	1	1	

I.e., the results of the squares are equal to each other and represent the number 144. In the Haar-Krestenson's codes, these operations are performed on the difference-modular matrices (4) and logic modules of the squares (5) for each module P_i (Fig. 11). The result is the following Haar-Krestenson's code: 0 0 1 1.

This property of Haar-Krestenson's code squares makes it possible to simplify the implementation of two consecutively connected components of the Haar-Krestenson's special processor by directly using the source direct and complementary codes of the difference-modular matrixes (4) and replacing the logical elements "OR" by the corresponding "AND-NOT" elements based on modular squares (5) (Fig. 11).

Therefore, the total delay of signals in the developed special processor for determining the squares of modular differences between two input analog signals, regardless of the digit of the input numbers, is: $\tau_2 = 4\nu + 2\nu + 1\nu + 1\nu = 8\nu$ (ν is time delay of the signal in one microelectronic logic gate). I.e., at the clock frequency of the FPGA valves of 500 MHz, the formation of the source codes of the difference squares will be carried out at a frequency of 125 MHz, which, in comparison with the known devices for determining the square of differences in Rademacher's basis, when encoding the input numbers in the ranges 8, 10, 12, 16, 24 performance is respectively 10.7; 13.25; 15.75; 20.75; 28.75 times.

VI. METHOD AND MEANS OF MONITORING TECHNOLOGICAL PROCESSES AND COMMUNICATION INTERACTION WITH THE OPERATOR IN THE ENVIRONMENT OF THE CYBER-PHYSICAL SYSTEM

Advances in microprocessor technology, theory of formation, transmission and processing of structured data (SD) provided creation and successful implementation of interactive real-time computer systems that can monitor, diagnose and control complex multiparameter processes and industrial objects. Powerful theoretical base of measurement data processing on the basis of CAD and formation of structured information flows in the form of such frame interactive systems as: control object (CO), operator, computer network (CN), environment of monitoring data registration (MDR) and systems of control and automation (SCA) are used in the process of development of these systems.

Development of the theory and integrated image display methods of an operator of normal, abnormal, emergency and pre-emergency states of the CO is a significant issue of improvement and efficiency increasing of monitoring data (MD) application. It particularly applies to explosive and environmentally hazardous COs, such as: mobile vehicles and aircrafts, nuclear power plants, oil and gas production, transportation, processing and storage equipment, mines, chemical and metallurgical enterprises.

Amount, structural complexity of monitoring information flows and a hazard of abnormal or emergency states of COs increase when the production technology becomes more complex due to the use of controlled microprocessor means. At the same time, the role and responsibility of computer system operators also increase in order to ensure equivalently rapid subjective response to CO norm deviation and to make quick right decisions to eliminate them. So, the development of the theory and SD formation of image-cluster monitoring of complex stationary multiparameter object states are significant issues today.

CO entropic states can be identified on the basis of their parameters which are defined according to the operator's frame and their structuralized image-cluster model is created according to the following expression [6]: $X_{CO}=F(\{x_i\}, \{x_j\}, S_{CO}, M_x, M_j, M_v, D_x, \delta_x, R_{xx}, R_{xy}, S_w, L_i, \rho_{ij}, S_{ij}, P_{ij}, I_x)$, where $\{x_i\}$, $\{x_j\}$ are arrays of digitized monitoring data of CO parameters; S_{CO} is semantic, information and technological CO states; M_x, M_j, M_v is selective, moving and weighted mathematical expectation; D_x, δ_x is dispersion and standard deviation; R_{xx}, R_{xy}, is autocorrelation and cross-correlation functions; S_w, are COs parameters spectra in various theoretical and numerical bases; L_i – logical and statistic information models (LSIM), $i \in \overline{1..5}$; ρ_{ij}, S_{ij}, P_{ij} are matrixes of cross-correlation coefficients, cluster model of probability transitions and entropic states; I_x is entropy correlative measure of CO state.

Further structuring of data monitoring and development of CAD method of image-cluster display of normal and abnormal CO states on the screen of the operator's monitor is an effective solution of image-cluster model building.

As an example of image-cluster display of superstructure monitoring of quasi-stationary CO is the forming of dynamic slides which are stylized and close to the human face features with cyclic renewal in real time in discrete boundaries of 0,8–0,2s that meets the ergonomics requirements of information perception by the subject – operator (Fig. 14).

Static or dynamic two-level and coloured characters that display the dynamics of structured data arrays are formed in particular points of the monitor. This is the principle of creating image-cluster model. Image-cluster models (a, b, c) correspond to the CO states – normal, abnormal (pre-emergency) and dangerous-alarm status.

Image-cluster model restructuring occurs in case of structured data coefficient change due to the particular positions of image-cluster model (Fig. 15).

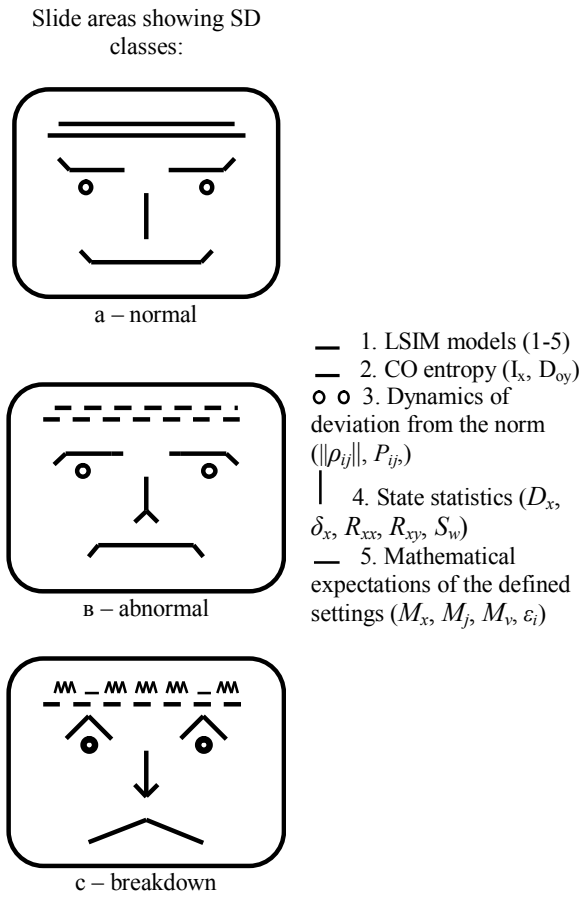

Fig. 14. Super-structured image-cluster models of CO

The task of enhancing the functionality for subject of law information neuro-model is realized by introducing into its structure a memory environment that accumulates and processes information and material flows that affect the intellectual attribute of a legal entity and influences its behaviour, as well as coefficients of significance.

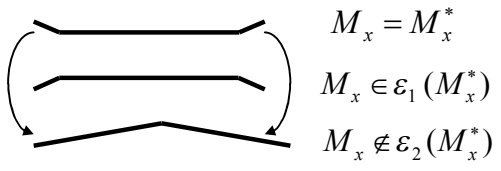

Fig. 15. Principle of image-cluster model attribute creation. M^*_x is setting of CO norm states

Formation of initial information and material flows of reaction of the intellectual attribute of the subject of law is described by the expression:

$$Z_i = \sum^{i} \beta_i; \;\; \beta_i = sign \sum^{i} \alpha_i \bullet w_i \qquad (10),$$

where w_j is one of the input information or material streams that act on the intellectual attribute (X, Y, D, G, I, M, T, S).

The structure that implements the information neuro-model of subject of law is shown in Fig. 16, where 1 is the intellectual attribute of the subject of law; 2 is external input information and material flows ($2_1 \div 2_9$); 3 and 4 are external relevant output information and material flows; 5 is multipliers; 6 is the adder; 7 is a form unit of a sign function logical unit; 8 is the memory environment; (β_x, β_y, β_a, β_i, β_m, β_g, β_s, β_t, β_n) are coefficients of significance of incoming communication interactions; α_j is the thresholds for the effects of the total weighted sums, according to the coefficients of external interactions, to which the entity's intellectual attribute responds; j is an arbitrary number of factors of each external interaction of the subject.

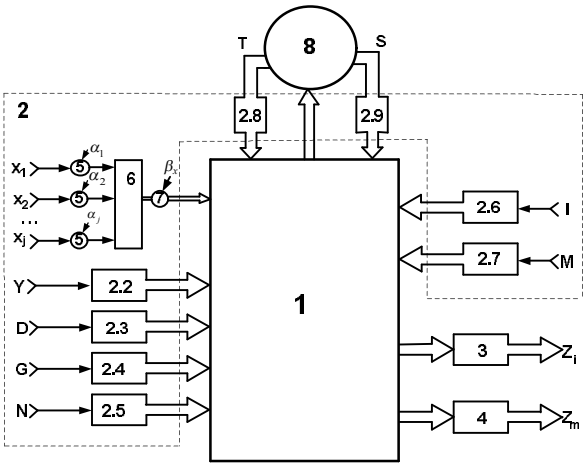

Fig. 16. Information neuro-model of subject of law

E.g., the following types of interactions: 2 is external input interactions: 2.1 – (x_1, x_2,...,x_j) are active random interactions; 2.2 – (y_1, y_2,...,y_j) are administrative, legislative interactions; 2.3 – (d_1, d_2,...,d_j) are reasonable economic interactions; 2.4 – (g_1, g_2,...,g_j) are factors of life survival; 2.5 – (n_1, n_2,...,n_j) are unforeseen, inactive or predicted unidentified flows of external interactions; 2.6 – (i_1, i_2,...,i_j) are information interactions; 2.7 – (m_1, m_2,...,m_j) are material interactions; 2.8 – (s_1, s_2,...,s_j) are functions of fear and evaluation of the result of their reaction to external information and material interactions; 2.9 – (t_1, t_2,...,t_j) are secret information that is not consciously or intentionally displayed in the original information and material flows of interactions; 3 and 4 are relevant information and material source external flows.

The structure of a neuro-model with advanced functionality is proposed by introducing a memory environment and processing the coefficients of significance of input information and material flows, as well as the formation of a neuro-threshold function at its outputs

The model developed can be used in the field of information law to formalize and identify the communication interactions of operators – subjects of law in the environment of computerized systems of

monitoring and management of industrial objects and with other entities in the environment of the information society.

VII. CONCLUSION

The fundamental foundations of the construction concept of cyber-physical systems, developed by prof. A.Melnyk are outlined in this paper. Systematic and generalized criteria for evaluation of structural, hardware, time and information-structural complexity of basic microelectronic components and software-hardware of cyber-physical systems are systematized and generalized. New effective schematic solutions for components of information-measuring and computing tools of cyber-physical systems are proposed, including: high-speed converters of analog-to-digital multifunctional measurement data encoding; an example of effective coding in the Haar-Krestenson's RGB-pixel color image. There is offered an effective encoding of measurement information for different accuracy classes sensors and refinement of communication protocols with increased frame identification reliability in the protocol structure.

A new information technology is proposed for the formation of data exchange protocols at the signal level with detection and correction of errors in the data transmission process based on the Galois theoretical and numerical basis. There is given an example of the structural implementation and principles of converting analog signals and codes of a high-speed special processor that determines the Hamming distance according to the estimation of a squared Euclidean distance in Haar-Krestenson's basis, which performs computational operations with a delay of 8 micro clock signals. There is also proposed the method and means of monitoring technological processes and communication interaction with the operator in the environment of the cyber-physical system based on the functional state of the management object, application of the image-cluster and information neuromodel of the subject of the law.

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