TRANSFORMING AND PROCESSING THE MEASUREMENT SIGNALS

SERIES TERMINATION OF SINGLE-ENDED LVCMOS SIGNALS

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Abstract. For synchronous signals with fast edges traces on printed circuit boards are transmission lines, not just conductor connections. If the length of the PCB trace exceeds certain values, it is necessary to match its impedance with the signal source and/or receiver. Impedance mismatches would bring signal reflections from the source to the receiver and back through the transmission line. Such reflection or distortion of the signal is called "echo" or "ringing". It is shown in emissions and irregularities of the waveform, especially the rise and fall edge. In this article, practical guidelines for sequential termination of one-way signals are considered that would resolve such effects. The simulations were done for LVCMOS signals [1].

Key words: Single-ended signals, synchronous signals, impedance matching, rise/fall time, transmission line.

1. Introduction

The analysis of the wide range of synchronous signals in various applications reveals the different nature of the waveform depending on the system in which it is applied. The best example of distributed component design is the transmission line. A signal established at one end appears on the other end after a certain time. In this case, the effect of dispersion becomes visible, since the length of the electrical line exceeds approximately 10–20 % of the signal wavelength. A lumped system is known as a scheme of concentrated elements [2]. Most printed circuit boards (PCBs) can be modeled with lumped elements such as resistors, capacitors, inductors, and diodes. The distributed elements, such as transmission lines, can be modeled with concentrated elements. A perfect line possesses two significant characteristics. The first is its impedance (electrical resistance). The second is electrical length. Both of these line properties can be simulated with the appropriate elements and setting the suitable values. The impedance can be simulated as series resistance and small values of inductance and capacitance, which corresponds to the "parasitic" characteristics of the PCB trace. An electrical length could also be simulated as a set of a certain number of L and C elements [3].

It should be noted that the speed of signal propagation in any environment is limited, so there cannot be an ideal lumped system. It is a general approach to compare the PCB trace length with the effective edge length of the fastest clock and, based on this ratio, adopt whether the system can be considered as a lumped system. The effective length of the signal edge can be calculated as:

$$L = \frac{T_u}{T_d}, \qquad (1)$$

here L is the length of the rising edge, T_u is the rise time which can alter from 10 % to 90 %, T_d is the propagation delay per unit length.

For example, the propagation delay in an FR4 PCB trace ranges from 5.5 to 7.1 *ps/mm* [4]. Assuming that T_d = 6.4 *ps/mm* the effective length of a 1 ns rising edge is 156.25 mm.

Based on the rise/fall time, a PCB trace can be considered as lumped if its length is less or equal to one-sixth (L/6) of the effective length of the signal edge. If only 20 % – 80 % rise/fall time is available a more appropriate way to determine whether a trace can be considered as lumped is the L/4 ratio. Those dependencies are not fully accurate, but they can be referenced to quickly determine whether the system is lumped. A lumped system does not require termination (additional resistors/capacitors equal to the PCB trace impedance to reduce signal reflection). For example, assuming a clock signal with 1ns rise time (10-90 %) and FR4 board material traces longer than 26 mm should be treated as a distributed system, and termination should be applied.

The oscillator rise/fall time numbers should be selected from the datasheet depending on the load value. Mandatory to pay attention to which rise/fall time 10-90 % or 20-80 % is shown in the datasheet for the selected device.

2. Drawbacks

For receivers requiring rising edges less than 0.5 ns at a frequency higher than 100 MHz, series termination is not recommended. Such a type of termination does not change the amplitude of the signal or remove the alternating current (AC) component of the signal. In those systems, the placement of passive elements on the PCB and the signal rise/fall time is more critical. Moreover, for one signal

source with several receivers, a better waveform would be created by combined types of termination.

3. Goal

Based on the simulation of the impedance mismatch of the source and the transmission line, justify the expediency of the correctly located series termination of single-ended signals.

4. Series termination of LVCMOS signals

The practical aspect can be explained when a clock driver sends an edge into the transmission line, the edge reaches the load after a certain delay. If the impedance of the load differs from the impedance of the transmission line, then part of the signal is reflected from the load to the source. Misalignment on the source side produces part of the reflected signal to be reflected to the load (round-tip reflection). Applying the termination would eliminate such kind of effects. There are four types of terminate a transmission line: series, parallel, Thevenin, and AC (for alternating current). Each can be applied to minimize reflections and improve signal integrity [5-9].

This article describes the most common in practice series termination. Its advantage lies in its simplicity it requires only one resistor. The disadvantage of this method is the increase in the rise/fall time of the signal. The series termination improves signal quality by eliminating secondary reflections from the source. The other three termination methods eliminate reflections by creating additional load on the receiver side. Series termination for one source and one receiver of a single-ended signal is introduced in Fig. 1.

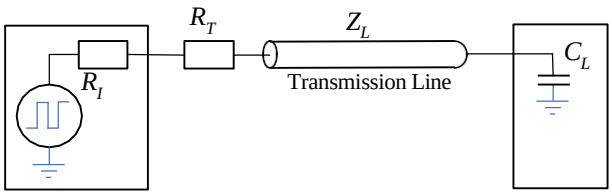

Fig. 1. Series termination for one source and one receiver of single-ended signal

For proper impedance matching the output impedance of the clock driver R_I plus series termination resistor R_T should be equal to the trace impedance Z_L, i.e.:

$$R_I + R_T = Z_L \quad (2)$$

It means that the value of the termination resistance can be determined based on the value of the internal resistance of the signal source for specific PCB traces. For most applications recommended value of R_T varies from 5 Ohms to 30 Ohms.

To illustrate the effect of termination on the waveform of the LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) signal the simulation for the oscillator SiT8008 [10]. For simulation, the selected Input/Output Buffer Information Specification (IBIS) model with a supply voltage of 3.3 V, a transmission line impedance of 50 Ohms, and a line length of 20 mm (Fig. 2). The load here and in other subsequent simulations is an input with an equivalent capacitance of 5 pF. For the numerical evaluation, it utilizes signal rise time T_R (0–100 %): from 0V to a stable level of 3.3V [1].

If the same circuit is simulated with an additional series resistor placed as close as possible to the signal source, then depending on its value the LVCMOS waveform would change as shown in Fig. 3.

The simulation visualizes that series termination with a 25 Ohm resistor gives a correct waveform without overshoots and spurs, but it also reduces the signal rise time. The value of the series resistor should be calculated more precisely. Based on the datasheet, we determine that the typical output impedance of the SiT8008 [9] device is 27.8 Ohm. Substituting the trace impedance and the output impedance into Equation 2, we calculate the value of the termination resistor R_T = 50 Ohm – 27.8 Ohm = 22.2 Ohm. If we would select this value for simulation, the signal rise time would be further reduced to 3.2 ns.

An additional factor worth analyzing is the length of the transmission line. In practice, for lumped systems, termination works and produces an ideal waveform. However, increasing the length of the EVB trace would necessarily lead to signal beating (distortion). Such behavior reflects the imperfection of the board and the impossibility of installing a termination resistor directly on the oscillator output pad (on the board). Thus, there is a path (of non-zero length) connecting the termination resistor with the signal source. These factors can be estimated if we simulate a non-ideal board with a termination resistor located at a certain distance from the LVCMOS signal source. The simulation results of the LVCMOS signal with a series termination of 22.2 Ohms refer to Fig. 4, with the series resistor placed 0.5 mm from the source for different transmission line lengths. A minor change in the termination resistor value would not eliminate the effects. It can only be done if the rising edge is slowed down (in the range of 10-90 %) enough and the system becomes lumped. In a specific application, it is necessary to find a compromise between the length of the transmission line and the signal waveform.

Another option for series termination that can be considered is placement – changing the position of the resistor over the PCB trace. This should change the signal waveform. However, such an approach does not improve the signal waveform it creates irregularities on the

signal edges. This method can be recommended only if it is impossible to implement the previously presented solution. Let us consider Fig. 5 to verify this statement. The waveforms for the series termination resistor placed 0.5 mm from the signal source, in the middle between the source and the signal receiver, and 0.5 mm from the receiver, are different. For all signals shown in Fig. 5, the total length of transmission lines is 50 mm.

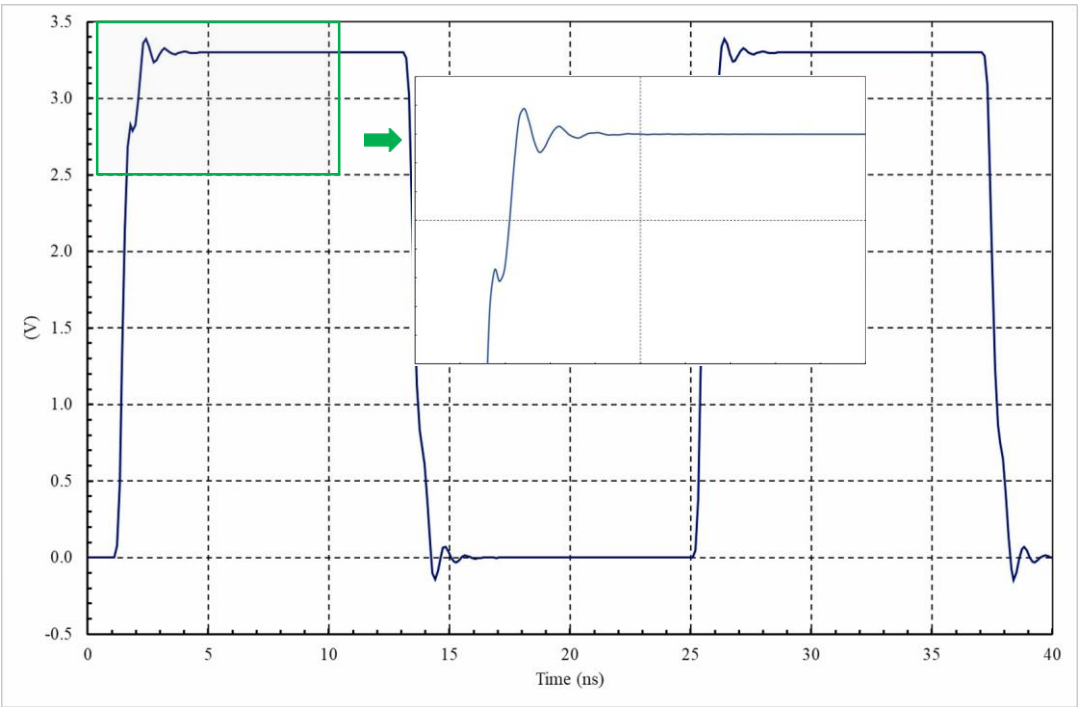

Fig. 2. Simulation of LVCMOS waveform without termination $T_R = 5.6$ *ns*

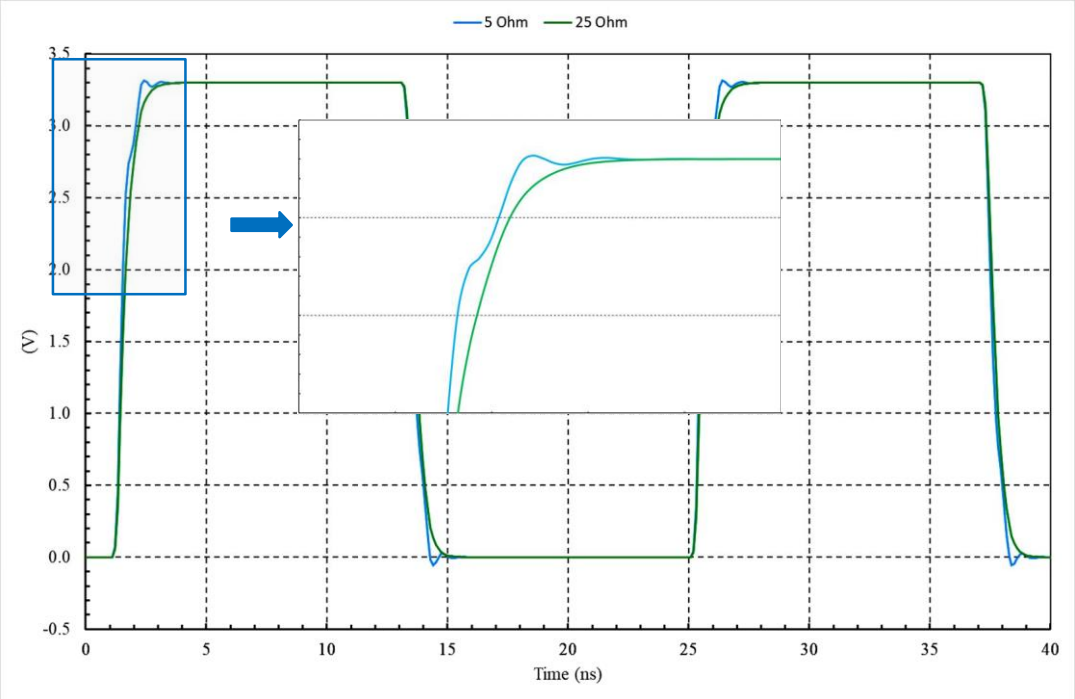

Fig. 3. Simulation of LVCMOS waveform with series termination
For $R_T = 5$ *Ohm* $\rightarrow$ $T_R = 3.7$ *ns ; for* $R_T = 5$ *Ohm* $\rightarrow T_R = 3.3$ *ns*

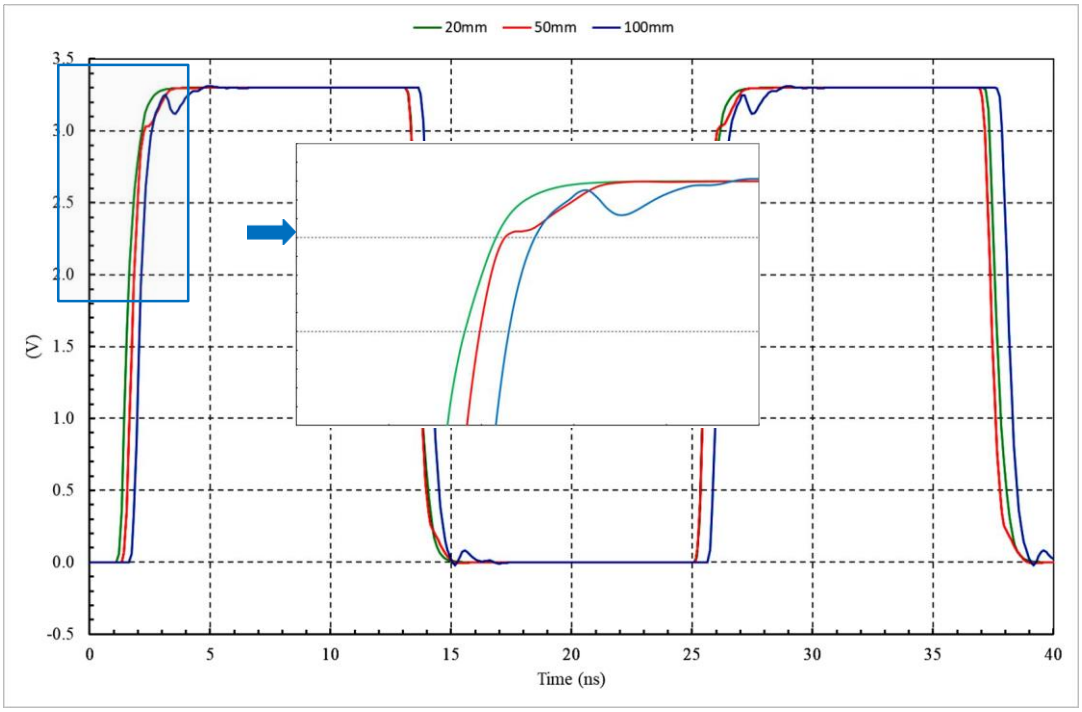

Fig. 4. Simulation of LVCMOS waveform with series termination 22.2 Ohm for different transmission line lengths Trace length 20 mm →$T_R = 3.2$ ns ; 50mm → $T_R = 3.9$ ns ; 100mm→ $T_R = 4.5$ ns

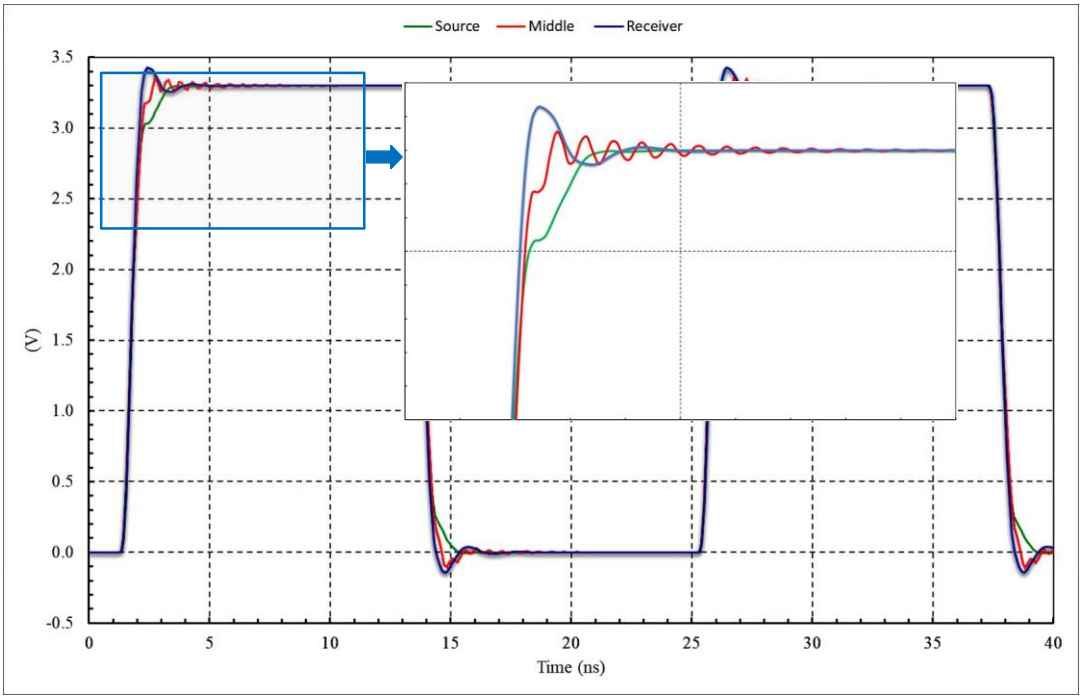

Fig. 5. The LVCMOS waveform depends on the placement of the termination resistor: Source – 0.5 mm from the signal source $T_R = 3.9$ ns ; Middle – in the middle between the source and receiver of the signal $T_R = 8.1$ ns ; Receiver – 0.5 mm from the signal receiver $T_R = 4.7$ ns

The minimum rise time, for this length of the transmission line, is received for the minimal distance between the signal source and the series termination resistor. This is the reason for placing the termination resistor as close as possible to the signal source. However, the complexity of PCBs, or the limitation in geometric dimensions, can implement their corrections in placement.

5. Conclusions

If there exists an impedance mismatch between the load and the transmission line, a part of the signal reflects from the load towards the source correspond- ingly distorting the LVCMOS waveform. The series termination of the oscillators eliminates this effect. It is an addition of a series resistor, the value of which is based on compensating the difference between the out- put resistance of the oscillator and the transmission line impedance. Selecting the appropriate resistor value, we would get the fastest rise time.

The results of series termination simulations dem- onstrate that the following factors can distort waveform:

- Incorrect value of the termination resistance – distorts the waveform and increases the rise/fall time.
- Incorrect resistor placement on the PCB – dis- torts the edges of the signal.
- Significant lengths of the transmission line dis- tort waveform even with the correct termination resistor value.

The application where optimal termination place- ment is impossible for any reason should be analyzed to find a compromise between the position and value of the series termination and how it affects the waveform. The Input/Output Buffer Information Specification (IBIS) or Simulation Program with Integrated Circuit Emphasis (SPICE) models can be applied for such simulations. Also, it is important to complete the correct simulation of the board trace and understand whether the system is lumped.

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