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RESEARCH AND DESIGN OF MULTIBIT BINARY ADDERS ON FPGA

Ihor Kogut[1], Volodymyr Hryha[1], Bohdan Dzundza[1], Liudmyla Hryha[1], Iryna Hatala[2]

[1]*Vasyl Stefanyk Precarpathian National University, 57, Shevchenko Str, Ivano-Frankivsk, 76018, Ukraine,*
[2]*Wayne State University, 42, Warren Ave, Detroit, 48202, USA.*
Authors' e-mail*: igor.kohut@pnu.edu.ua, volodymyr.gryga@pnu.edu.ua, bohdan.dzundza@pnu.edu.ua, liudmyla.hryha@pnu.edu.ua, iryna.hatala@gmail.com*

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***Abstract*: This paper provides an analysis of the system characteristics and functional capabilities of various types of adders for the high-speed component construction of arithmetic and logical devices in modern superscalar processors. The main features of parallel prefix adders (Sklansky, Brent Kung, Kogge Stone, Ladner Fisher, Han Carlson) and tree-like structures based on incomplete binary adders have been determined in this study. The structures of typical and improved incomplete binary adders have been shown and their complexity characteristics have been calculated as well. Various architectures (structures) of multi-bit adders have been built on the basis of well-known and improved binary half-adders. Analytical expressions for calculating the hardware and time complexity of the presented multi-bit adder structures have been obtained as a result. Schematic topological modeling of the improved half-adder based on CMOS-structure has been carried out and its topology has been produced in a specialized environment. Models of multi-bit adders using hardware description language VHDL have been developed. Modeling and synthesis of the developed multi-bit adders on the Xilinx FPGA has been carried out. It has been established that when using the proposed improved structures of binary half-adders as part of a multi-bit adder, the hardware complexity has been reduced by 1.7 times and the computational performance was increased by 3 times.**

***Index Terms*: Binary half-adder, FPGA, CMOS-structure, topology, synthesis, ALU.**

I. INTRODUCTION

In digital computing, binary addition is the most common operation used, which lays the basis for arithmetic operations of binary multiplication, division, exponentiation and other special operations, especially multiplication with accumulation, trigonometric operations, etc. [1].

Multi-bit binary adders (MBA) are widely used in computer devices, arithmetic logic unit (ALUs), matrix and multilayer multipliers, microcontrollers, and specialized scalar processors of computer-based measurement and telecommunication systems [1-4].

MBA are functionally and structurally divided into the following classes: linear (cascade, chain) without structural branches; adder-accumulator with memory; pyramidal adders; adders with accelerated transfers; vertically organized adders and parallel prefix adders [5,6].

Important criteria for the efficiency of multi-bit binary adders (MBA) are ensuring minimum hardware complexity and maximum performance with minimum delay of sum bit signal production and end-to-end transfers. Other important parameters of MBA components are the minimum structural complexity and functional completeness.

There are many different types of structures of binary one-bit full and half-adders that are a part of the MBA.

Thus, an in-depth research in the system characteristics of MBA and its single-digit components not only as a separate structure, but also as a functional component in different adder positions is an urgent scientific and engineering task.

II. LITERATURE REVIEW AND PROBLEM STATEMENT

Depending on the task, there are three main types of binary half-adders (BHA) [1,4]: BHA with single-phase direct inputs and outputs; BHA with single-phase inverse inputs and outputs; BHA with two-phase inputs and outputs.

Most commonly, single-phase binary half-adders with direct inputs and outputs are used in multi-bit binary adders.

The following papers [2,4] describe the classic structure of a binary half-adder, which contains a 2-input «AND» logic gate and a 2-input «Exclusive OR» logic gate. The structure of such half-adder is demonstrated in Fig. 1.

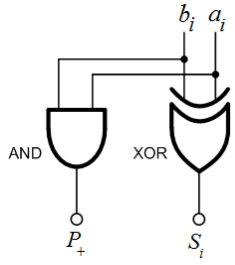

Fig. 1. Classic binary half-adder structure

It should be noted that the "Exclusive OR" logic gate internal structure consists of four NAND gates (Fig. 2).

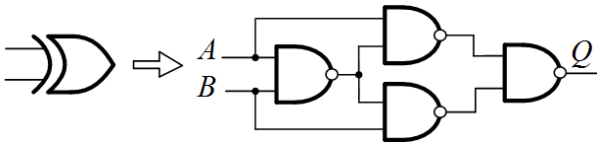

Fig. 2. «Exclusive OR» logic gate internal structure

As it can be seen in the Figure 2, the logic gate «Exclusive OR» has a hardware complexity of $A_{XOR} = 4$ (gates) and a time complexity of $t_{XOR}=3$ (microcycles).

Therefore, total hardware complexity of the classic half-adder will be $A_{CHA} = 5$ (gates), with the sum time complexity and the output transfer time being 3 and 1 microcycles, respectively.

Such system characteristics are redundant and do not provide an opportunity to maximize the performance of multi-bit binary adders as a part of ALU processors.

Thus, the sum bit computation is much slower than the carry bit computation, which results in a significant lag between the signals of half-adder of this type.

In a related study [4], an improved structure of a half-adder, which is built using «AND», «OR», «NOT» logic gates (Fig. 3), has been proposed.

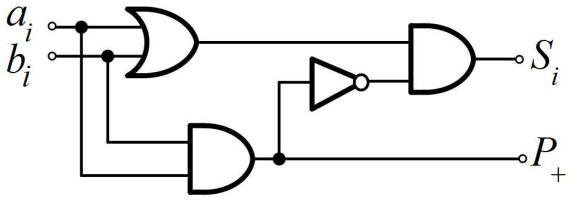

Fig. 3. An improved binary half-adder structure based on «AND», «OR», «NOT» logic gates

The hardware complexity of such improved binary half-adder will be $A_{CHA} = 4$ (gates), with the sum time complexity being 3 microcycles, and the output transfer time being 1 microcycle, which is very similar to the general system characteristics of a classical half-adder.

In the following paper [4], an alternative solution for the half-adder structure has been proposed, which is built based on «AND», «OR», «NAND», «NOT» logic gates (Fig. 4).

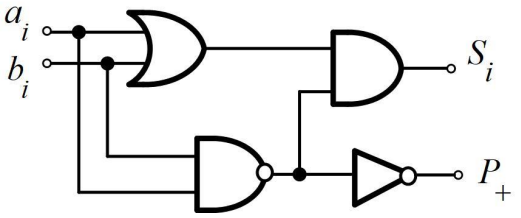

Fig. 4. An improved binary half-adder structure based on «AND», «OR», «NAND», «NOT» logic gates

The hardware complexity of such binary half-adder is $A_{HA} = 4$ (gates), with the sum time complexity and output transfer being 2 microcycles, enabling the circumvention of unnecessary delays in multi-bit structures.

Another improved variant of the binary half-adder structure based on «AND», «OR», «NAND» logic gates has been developed in a related research paper [7], minimaxing hardware and time complexity characteristics (Fig. 5).

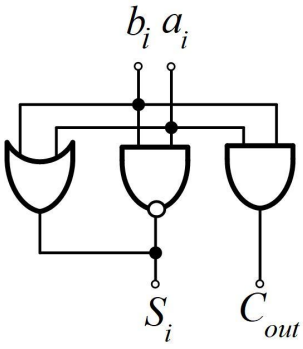

Fig. 5. An improved binary half-adder structure based on «AND», «OR», «NAND» logic gates

The hardware complexity of a previously developed binary half-adder will be $A_{HA}=3$ (gates), while the sum time complexity and output transfer is minimal and amounts to 1 microcycle.

The above mentioned binary half-adder works as follows. Applying values ($a_i=0$, $b_i=0$) to the half-adder inputs generates a «1» signal at the «NAND» logic gate output and a «0» signal at the «OR» logic gate output, which corresponds to the S=0 signal. Additionally, a "0" signal is produced at the «AND» carry bit logic gate output.

Switching values to ($a_i=1$, $b_i=1$) at the half-adder inputs produces a «0» signal at the «NAND» logic gate output together with a "1 signal at the «OR» logic gate output, which corresponds to the S=0 signal, respectively a «1» signal is produced at the «AND» carry bit logic gate output.

Finally, applying values ($a_i=1$, $b_i=0$ and $a_i=0$, $b_i=1$) to the half-adder inputs produces «1» signal at the «NAND» logic gate output alongside with the «1» signal at the «OR» logic gate output, which corresponds to the S=1 signal. At the same time, a «0» signal is produced at the «AND» carry bit logic gate output.

The hardware and time complexity reduction of an above-mentioned half-adder occurred due to the simplification of the «Exclusive OR» logic gate structure by the usage of a «Conductive AND» logic gate, which results from combination of «NAND» and «OR» logic gates.

This is due to the fact that the use of logic gate implemented with emitter-coupled logic (ECL) microelectronic technology implies the presence of transistors at the «NAND» and «OR» gate outputs, which allows to combine their outputs without any functional loss and implementing the «Conductive AND» gate [7].

A schematic topological modeling of the improved half-adder structure based on «AND», «OR», «NAND» logic gates was carried out at the electronic level using the LT-SPICE package [8].

The electrical diagram of the improved binary half-adder (Fig. 5) using CMOS-structures is showcased in the Fig. 6.

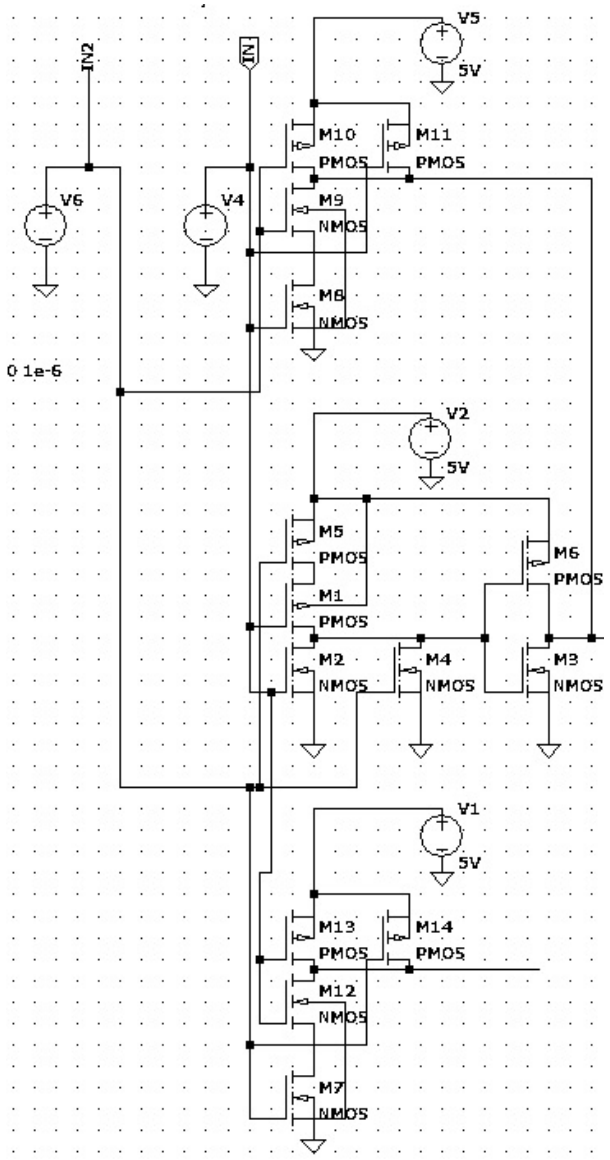

Fig. 6. Electrical diagram of an improved half-adder based on «AND», «OR», «NAND» logic gates

The proposed improved half-adder electrical diagram contains 14 MOS transistors («OR» logic gate - 6 transistors, «AND» logic gate - 4 transistors and «NAND» logic gate are 4 transistors).

The results of functional modelling of an improved half-adder based on «AND», «OR», «NAND» logic gates are presented on the Fig. 7.

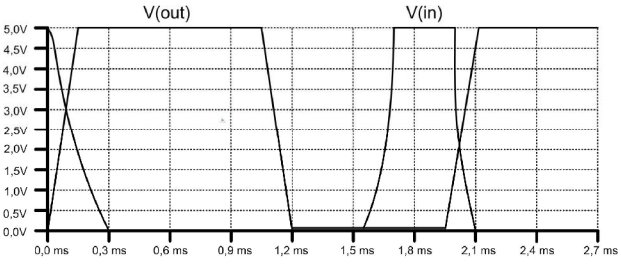

Fig. 7. Functional modeling diagram of the improved half-adder electrical circuit

On the resulting functional diagram, the uniform formation of a low signal level - log. «0» (V=0V) and high signal level - log. «1» (V=5V) of the binary half-adder can be observed.

The topology of the improved NS in the MicroWind package, presented in the Fig. 8, was based on the basic matrix cell of the uncommitted logic array (ULA). P-channel MOS transistors are implemented in an n-type conductivity pocket with polarized bias by the supply voltage. N-channel MOS transistors are implemented in p-type conductivity substrate.

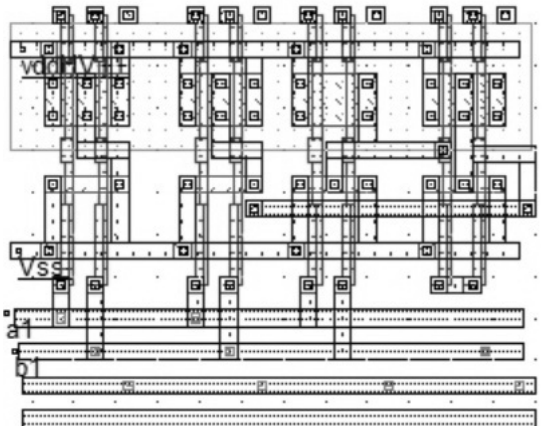

Fig. 8. Improved half-adder topology

The output inverter of the 2I circuit is implemented as a double cascade of two inverters.

In related studies [5,6], the structures of parallel prefix adders are described, which ensure high performance in summation delay by implementing separate combinational circuits for the sum and carry propagation. These parallel prefix adders include: the Sklansky Adder, Brent-Kung Adder, Ladner-Fischer Adder, Kogge-Stone Adder, Han-Carlson Adder, H. Ling Adder, and others.

In parallel prefix adders, three stages are required to compute the result: preprocessing, carry generation, and sum generation.

A significant drawback of parallel prefix adders is their high hardware complexity, which significantly increases the power consumption of the chip when dealing with streams of multi-bit data (greater than 64 bits).

Therefore, the development of components for multi-bit adders based on half-adders, which exhibit minimax characteristics in terms of hardware cost and performance is of the utmost importance.

III. SCOPE OF WORK AND OBJECTIVES

The development of high-performance computing systems is a relevant task in today's environment of rapidly increasing demand for high-speed multi-bit ALU components used in the field of artificial intelligence. Herewith, the investigation of the system characteristics of both known and improved half-adder structures, which will serve as the foundation for building multi-bit binary addition structures, is an important task to solve.

The main objective of this paper is to research and design high-speed multi-bit pyramid-like adders on FPGAs for further application in cyber-physical systems [9].

This article uses the materials and results obtained by the authors during the research work "Multifunctional sensor microsystem for non-invasive continuous monitoring and analysis of human biosignals" state registration number 0124U000384 dated 01.01.2024, which is carried out at the Department of Computer Engineering and Electronics, of Vasyl Stefanyk Precarpathian National University in 2024-2026.

IV.RESEARCH AND DESIGN OF PYRAMID-LIKE MULTI-BIT BINARY ADDERS

Fig. 9 shows the structure of a 4-bit pyramid adder built on the basis of a half-adder [10-12].

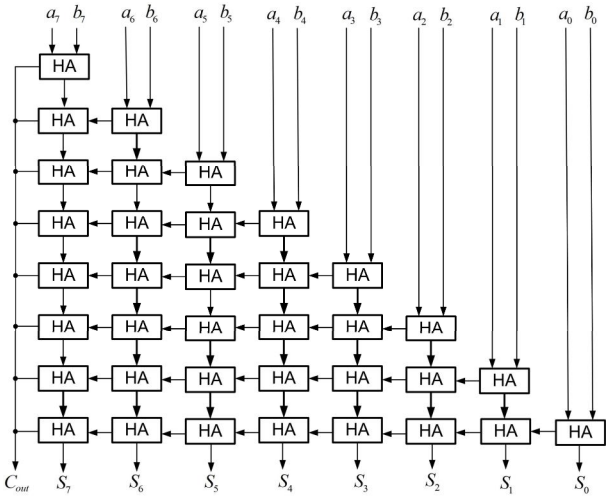

Fig. 9. Structure of a 4-bit pyramid adder built on the basis of a half-adder

The hardware complexity of this type of pyramid binary adders is calculated according to the following formula:

$$A_{PBA} = \frac{m^2 + m}{2} \times A_{HA}, \quad (1)$$

where, A_{HA} - hardware complexity of a half-adder, m - bit-length of the input data.

For example, with $m = 8$ using classical half-adders (A_{HA}=5), $A_1 = \frac{8^2 + 8}{2} \times 5 = 180$ (gates).

When using improved half-adders (A_{HA}=3), $A_2 = \frac{8^2 + 8}{2} \times 3 = 108$ (gates).

Thus, the hardware complexity of an 8-bit pyramid-like binary adder will be 1.7 times lower when using improved half-adders.

Table 1 presents the obtained results of hardware complexity for pyramid-like binary adders of different bit-lengths when using classical and improved half-adders.

Table 1

Pyramid-like MBAs hardware complexity results

MBA bit-length	Classical HA gate number (A_1)	Improved HA gate number (A_2)
8	180	108
16	680	408
32	2640	1584
64	10400	6240
128	41280	24768
256	164480	98688
512	656640	393984

The time complexity of this type of pyramid-like multi-bit binary adder is calculated according to the following formula:

$$t_{PBA} = m \times t_{HA}, \quad (2)$$

where, t_{HA} - time complexity of a half-adder, m - bit-length of the input data.

For example, with $m = 8$ using classical half-adders (t_{HA}=3), $t_1 = 8 \times 3 = 24$ (microcycles).

When using enhanced half-adders (t_{HA}=1), $t_2 = 8 \times 1 = 8$ (microcycles).

Thus, the time complexity of an 8-bit pyramid-like multi-bit binary adder will be 3 times greater when using improved half-adders.

Table 2 shows the obtained results of time complexity for pyramid-like multi-bit binary adders of different bit-lengths when using classical and improved half-adders.

Table 2

Pyramid-like MBA time complexity results

MBA bit-length	Classical HA time complexity (t_1)	Improved HA time complexity (t_2)
8	24	8
16	48	16
32	96	32
64	192	64
128	384	128
256	768	256
512	1536	512

An effective solution for reducing hardware complexity and improving the speed of this class of adders is to combine them with structures of smaller bit-lengths.

For example, when an 8-bit pyramid-like adder with reduced hardware complexity is required, it is preferable to implement the structure shown in Fig. 10.

In the presented structure of the 8-bit composed pyramid-like adder based on two m = 4-bit structures, full one-bit adders with an inverted carry input are used [13]. The full binary adder proposed in [13] contains 7 logic elements. The presence of inverted carry-in/out connections in such an adder prevents its use as a component for the serial connection of two 4-bit (or, in general, m-bit) pyramid-like adders.

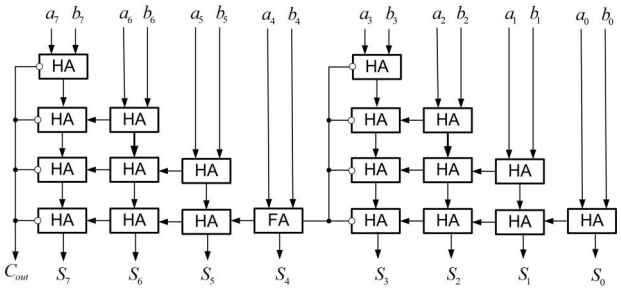

Fig. 10. Structure of a 2m-bit composed pyramid-like adder based on two m = 4-bit structures

Therefore, an inverter has been added to its structure (Figure 11), which ensures the generation of carry signals ($\overline{C_{in}} \rightarrow C_{out}$).

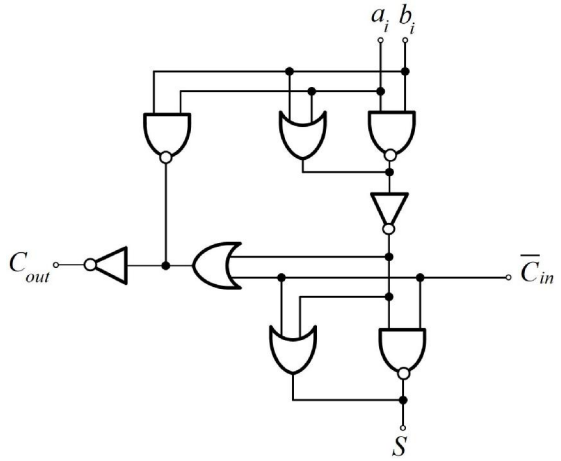

Fig. 11. Full one-bit binary adder with an inverted carry input structure

The hardware complexity of such a composed pyramid-like multi-bit binary adder is calculated using the following formula:

$$A_{CPMBA} = 2 \times (\frac{(m/2)^2 + m/2}{2} \times A_{HA}) + A_{FA}, \quad (3)$$

where, A_{HA} - hardware complexity of a half-adder, A_{FA} - hardware complexity of a full binary adder, m - bit-length of the input data.

For example, with $m = 8$ using classical half-adders, the hardware complexity is,

$$A_3 = 2 \times (\frac{4^2 + 4}{2} \times 5) + 8 = 2 \times 58 = 116 \text{ (gates)}.$$

When using improved half-adders, the hardware complexity is,

$$A_4 = 2 \times (\frac{4^2 + 4}{2} \times 3) + 8 = 2 \times 38 = 72 \text{ (gates)}.$$

Thus, the hardware complexity of an 8-bit composed pyramid-like multi-bit binary adder will be 1.6 times lower compared to the classical multi-bit binary adder.

Table 3 shows the obtained results of hardware complexity for the composed multi-bit binary adder of different bit-lengths when using classical and improved half-adders.

Table 3

Composed pyramid-like MBA hardware complexity

MBA bit-length	Classical HA gate number (A_3)	Improved HA gate number (A_4)
8	108	68
16	368	224
32	1368	824
64	5288	3176
128	20808	12488
256	82568	49544
512	328968	197386

When comparing the hardware complexity of the classical pyramid-like multi-bit binary adder with the composed multi-bit binary adder, a linear decrease in hardware complexity as the bit-length increases can be observed. For example, at m=128, the hardware complexity of the composed multi-bit binary adder will be 1.7 times lower compared to the classical structure.

The time complexity of such a composed pyramid-like multi-bit binary adder is calculated using the following formula:

$$t_{CPMBA} = (\frac{m}{2} \times t_{HA}) + t_{FA}, \quad (4)$$

where, t_{HA} - time complexity of a half-adder, t_{FA} - time complexity of a full binary adder, m - bit-length of the input data.

For example, with $m = 8$ using classical half-adders, the time complexity is, $t_3 = (4 \times 3) + 3 = 15$ (microcycles).

When using improved half-adders, the time complexity is, $t_4 = (4 \times 1) + 3 = 7$ (microcycles).

Table 4 demonstrates the obtained results of time complexity for pyramid-like multi-bit binary adders of different bit-lengths when using classical and improved half-adders.

Table 4

Composed pyramid-like MBA time complexity

MBA bit-length	Classical HA time complexity (t_1)	Improved HA time complexity (t_2)
8	15	7
16	27	12
32	51	19
64	99	35
128	195	67
256	387	131
512	771	259

When comparing the time complexity of the classical pyramid-like multi-bit binary adder with the composed multi-bit binary adder, a linear increase in time complexity as the bit-length increases can be observed. For example, at m=128, it will be 2 times greater compared to the classical structure.

V. MBA MODELING AND SYNTHESIS USING FPGAs

The development of multi-bit binary adders of the studied types was carried out using the Verilog hardware description language within the Active HDL SE integrated environment [14].

Fig. 12 demonstrates the functional simulation diagram of a 128-bit composed pyramid-like multi-bit binary adder.

This diagram shows the transmission of 128-bit integer binary values to the inputs of A and B. The output Q produces the 128-bit addition result.

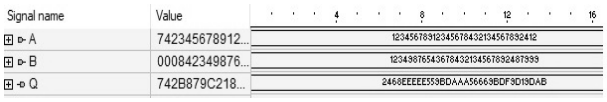

Fig. 12. Functional diagram of a 128-bit composed pyramid-like multi-bit binary adder operation

The synthesis of the studied MBA class was performed on the Artix-7 FPGA family, specifically the XC7A100TCSG324-1 chip from Xilinx.

Fig. 13 showcases a zoomed-in view of a FPGA chip area where the implementation of the 128-bit composed pyramid-like multi-bit binary adder structure took place within the Vivado Design Suite CAD software.

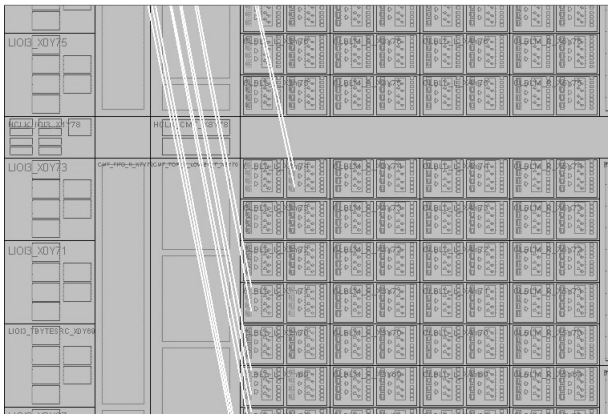

Fig. 13. 128-bit composed pyramid-like multi-bit binary adder implementation on the FPGA chip within the Vivado Design Suite

As a result of the composed pyramid-like multi-bit binary adder synthesis and implementation, 1230 out of a 63400 total available LUTs were utilized on the specified FPGA chip.

Table 5 presents the synthesis results for th classical and composed 128-bit pyramid-like multi-bit binary adders on the Artix-7 FPGA family using one-bit half-adder improved components.

Table 5

Pyramid-like MBA FPGA synthesis results

MBA bit-length	Classical MBA (LUT usage)	Composed MBA (LUT usage)
128	250	143

Based on the data, it can be concluded that 128-bit composed pyramid-like MBA implementation requires less than half the hardware of that needed for classical MBA implementation.

VI.CONCLUSION

This work presents the key application areas of multi-bit binary adders, integral components of arithmetic-logic units in processors. A detailed analysis of both traditional and improved half-adder components is provided, along with an evaluation of their system characteristics. Circuit-level and topological modeling of the improved half-adder based on CMOS structures was conducted. Additionally, the design and simulation of a 128-bit composed pyramid-like multi-bit binary adder were performed using the Verilog hardware description language. The synthesis of the composed pyramid-like adder on an FPGA using the Vivado CAD tool demonstrated a twofold reduction in hardware complexity and a twofold improvement in performance compared to the classical binary adder, confirming theoretical predictions.

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Igor Kohut, D. Sc, was born in Zelene village of Husiatyn district, Ternopil region, in 1953. He graduated from Lviv Polytechnic Institute in 1967. Ph.D. Solid State Electronics at Lviv Polytechnic Institite (1993), and his Doctor of Technical Sciences Degree in Electrical and Computer Engineering at Lviv Polytechnic University in 2010. He is the author of more than 250 scientific papers, including 50 copyright certificates for inventions and patents of Ukraine, 1 monograph and textbooks. Research interests: research and development of advanced element base for computing, specialized computer systems for control systems, sensor electronics, microsystems-on-a-chip based on advanced microelectronic technologies of large and ultra-large integrated circuits with silicon-on-insulator structures, including their three-dimensional architectures.

Volodymyr Hryha, PhD, was born in Nadvirna, Ivano-Frankivsk region in 1982. He was an engineering of Computer Systems. at Lviv Polytechnic University, Ukraine (2004). He received Ph.D. in Technical (Computer) Sciences in 2015 at Ternopil National Economic University.

He holds the title of Associate Professor of Department of Computer Engineering and Electronics of Faculty of Physics and Technology of Vasyl Stefanyk Precarpathian National University. He is the author of more than 150 papers (of which 25 patents of Ukraine). His main Areas of Research Interest are the design of specialized computer systems, FPGA, spatial-temporal graphs, Hardware Design Language, Programmable systems on the Chip, Internet of Things.

Bogdan Dzundza, PhD, was born in Bodnariv village, Kalush district, Ivano-Frankivsk region in 1982. 2004 – 2007 postgraduate studies at Vasyl Stefanyk Precarpathian National University, specialty Solid State Chemistry. In 2008 he successfully defended his thesis and received a PhD. He is a co-author of ten textbooks, two monographs, more than 130 publications in professional scientific journals, and has participated in many international scientific conferences. Research interests: studying the physical properties of semiconductor thin films and nanostructures (pure and doped materials, solid solutions, and multicomponent semiconductor compounds), thermoelectric and photovoltaic semiconductor materials development of automated laboratory research systems computer science, microcontroller systems and the Internet of Things.

Liudmyla Hryha, was born in Shepetivka, Khmelnytskyi region, in 1986. She was an engineer in the field of electronics and telecommunications. Lviv Polytechnic University, Ukraine (2008). Her main Areas of Research Interest are the design of specialized computer systems, databases, components computer system, sensor electronics, Programmable systems on the Chip, Internet of Things.

Iryna Hatala was born in Ivano-Frankivsk. She is a PhD student in the Physics and Astronomy Department at Wayne State University. Over the past three years, Iryna Hatala has worked as a graduate teaching assistant for five different classes within the Physics and Astronomy Department, including three of the introductory physics courses for undergraduate students. Research interests: physics and astronomy, condensed matter physics, studying the physical properties of semiconductor thin films and nanostructures (pure and doped materials, solid solutions, and multicomponent semiconductor compounds).