MEANS FOR MEASURING THE ELECTRIC AND MAGNETIC QUANTITIES

IMPROVING THE PSRR PARAMETER IN THE LINEAR VOLTAGE REGULATOR CIRCUIT

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Abstract. The article describes methods for improving the output parameter of a linear voltage regulator – the power supply ripple rejection (PSRR) coefficient. A simulation was conducted using LTSpice software with SPICE models of the differential amplifier elements and the p-channel transistor.

Keywords: PSRR, Linear voltage regulator, Low dropout regulators, LTspice Simulation program, Compensation.

1. Introduction

In modern electronic systems, the high quality of image sensors, accelerometers, magnetometers, or biosensors is considered critical for ensuring the accuracy, speed, and reliability of device operation. These sensors are widely utilized in smartphone cameras, automotive Advanced Driver Assistance Systems (ADAS), medical devices, industrial automation, and other fields. Since, in most cases, the output signals of sensors are analog and have low levels, any fluctuations or disturbances in the power supply system are capable of adversely affecting measurement accuracy, causing fluctuations, and leading to errors in data processing systems. To ensure the stable operation of such devices, power sources with minimal output voltage (current) fluctuations and a high level of suppression of these variations are required. Various methods are applied to achieve this, including the filtering of high-frequency noise using passive components (capacitors, inductors), the use of switching voltage regulators, which provide high conversion efficiency, and linear voltage regulators (LDOs). Despite the high efficiency of switching regulators, the high-frequency noise they generate is considered hazardous for sensitive analog systems, which are characterized by low levels of output voltage (current) fluctuations and ease of integration. In such cases, linear voltage regulators are recognized as the optimal choice. The use of linear voltage regulators with low dropout voltage across the regulating element is a simple and cost-effective method of regulating the system's supply voltage from a higher voltage source [1]. These regulators are used in a wide range of devices to regulate and control a lower output voltage supplied from a higher input voltage source [2]. Their primary advantages include minimal output voltage (current) fluctuations, ease of implementation due to the absence of a need for external inductors, which reduces the number of components and system dimensions, and rapid response to load changes, which is critical for sensors with uneven power consumption. The advantages of low dropout voltage include a lower minimum operating voltage, higher efficiency, and reduced heat dissipation [3]. The benefits of a small voltage drop across the regulating element (RE) allow for a reduction in the minimum operating voltage, an increase in efficiency, and a decrease in heat dissipation on the RE. One of the key parameters of LDOs that determines their effectiveness in systems with high-quality sensors is the power supply rejection ratio (PSRR). This parameter characterizes the regulator's ability to suppress input disturbances originating from the power source. A higher PSRR level ensures a lesser impact on the sensor from external disturbances, such as ripples from the switching power supply, voltage fluctuations due to transient processes, or electromagnetic interference from neighboring components.

2. The PSRR parameter and its role in modern electronic circuits

The power supply rejection ratio (PSRR) is regarded as one of the most critical parameters of linear voltage regulators, determining their ability to isolate the regulator's output voltage from unwanted variations in the input signal. This parameter reflects the effectiveness of suppressing disturbances such as fluctuations and voltage ripples that may enter the system through the power supply.

Generators of these disturbances may include switching voltage converters, unstable primary power sources, or external electromagnetic interference. If the regulator lacks sufficient ability to isolate the output voltage from these influences, significant operational issues may arise. For instance, in image sensors, photons are captured and converted into voltage values. The resulting voltage is then converted into a digital code processed by a computer [4].Therefore, from the moment photons are captured to the signal's processing by the computer, sen-

sors used in video or photo cameras or medical systems may begin generating signals with increased noise levels, reducing the quality of the acquired data.

PSRR is especially critical in low-voltage analog systems, where even minor voltage fluctuations significantly impact component accuracy. In such cases, a linear regulator with high PSRR is considered a key element ensuring stable and clean output voltage. Due to their simple construction, linear voltage regulators demonstrate high efficiency in suppressing high-frequency disturbances, which is particularly important for analog circuits where signal quality directly depends on voltage stability.

The PSRR value depends on the frequency of the disturbances: at low frequencies, regulators provide high suppression levels; however, as the frequency increases, PSRR effectiveness decreases. Consequently, developers focus on LDOs capable of maintaining high PSRR across a wide frequency range, ensuring reliable protection against interference generated by switching power supplies, which are commonly used in modern circuits.

Enhancing PSRR not only improves signal quality but also significantly simplifies the power supply filtering circuit.

PSRR is measured as the ratio of changes in the supply voltage to the corresponding changes in the device's output voltage, expressed by the following formula:

$$\mathrm{PSRR} = 20 \cdot \mathrm{Log}_{10}\left(\frac{\Delta V_{IN}}{\Delta V_{OUT}}\right), \mathrm{dB}\,. \qquad (1)$$

In the case of LDOs, this represents the measurement of output ripple compared to input ripple over a wide frequency range (typically from 10 Hz to 10 MHz) and is expressed in decibels (dB) [5]. Therefore, PSRR is considered one of the key factors in ensuring the stable operation of modern electronic circuits. By minimizing the influence of disturbances, linear regulators with high PSRR contribute to creating reliable and efficient systems that meet stringent requirements for accuracy, power consumption, and compactness.

3. Improving the PSRR characteristic of a linear voltage regulator

Ensuring a high power supply rejection ratio in linear voltage regulators requires meticulous design of the regulator's circuitry. One of the key approaches to enhancing PSRR is optimizing the performance of the regulator's amplification stage over a wide frequency range. To achieve this, methods such as "Lead-Lag" and "Miller compensation" are employed, which expand the capabilities of linear regulators and ensure a high level of noise suppression. Miller compensation is effective in stabilizing the negative feedback system, but in some designs, it may lead to oscillations in the feedback loop [6].

The use of Lead compensation in the internal circuit of a linear voltage regulator aims to ensure the stability of the feedback system. The primary goal of this method is to prevent undesirable oscillations and maintain a proper phase response. Lead compensation increases the system's phase margin by adding an "advancing" component to the phase response. This method enhances the regulator's transient response and dynamic performance.

Implementation is achieved through an RC circuit that introduces phase lead at specific frequencies. A stable loop generally requires at least a 20° phase margin (more is preferable) [7]. In internal amplifiers of voltage regulators, which generate the control signal for the regulating element operating as an active load on the transistor, Lead compensation ensures effective response to rapid load changes. The stability of the feedback loop with Lead compensation is achieved by compensating poles with zeros at frequencies:

$$f_{Lead} = \frac{1}{2\pi R_C C_C}, \mathrm{Hz}\,, \qquad (2)$$

f_{Lead} – zero frequency; R_C – the resistor in the compensation circuit; C_C –the capacitor in the compensation circuit.

To ensure system stability with feedback, the phase margin should be maximized. This is achieved by appropriately positioning the poles and zeros in the system's frequency response.

In an LDO circuit, the use of an output C_{LOAD} capacitor [8] with an internal equivalent series resistance (ESR) is mandatory. The ESR value determines the location of the poles and zeros in the feedback system's frequency response, affecting phase margin, stability, and LDO efficiency. ESR also impacts PSRR by influencing the filtering of power supply ripple.

An excessively low ESR value may limit high-frequency noise suppression, whereas an excessively high value deteriorates overall filtering. An optimal ESR value balances stability, low noise, and efficient regulator performance. Therefore, selecting an output capacitor with an optimal ESR value is crucial.

4. PSRR analysis in an LDO circuit using SPICE models

Fig. 1 illustrates the electrical schematic of an LDO, which consists of an error amplifier on a differential stage and a regulating element on the *p*-channel MOS transistor MOSP3.The differential stage is formed using transistors MOSN1 and MOSN2 along with a current source based on MOSN4. Transistors MOSP1 and MOSP2 are utilized as the active load of the differential stage. The error signal is applied to the input of the differential stage from the output voltage divider *R*1, *R*2.The amplified error signal is fed to the input of the RE on transistor MOSP3 to compensate for the error. Additional

control of the RE is provided by applying voltage to the gate of MOSN2. C_{LEAD} and R_{Lead} are components of Lead compensation. This configuration allows for the implementation of a simple linear voltage regulator with low dropout, an output voltage of 1.2 V, and a load current of up to 30 mA.

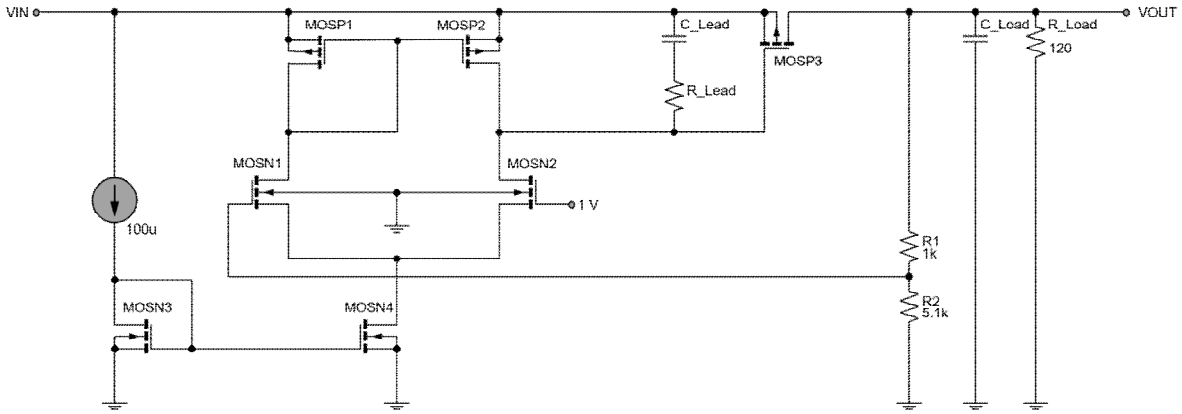

Fig. 1. Internal circuit of LDO based on operational amplifier and P-channel transistor

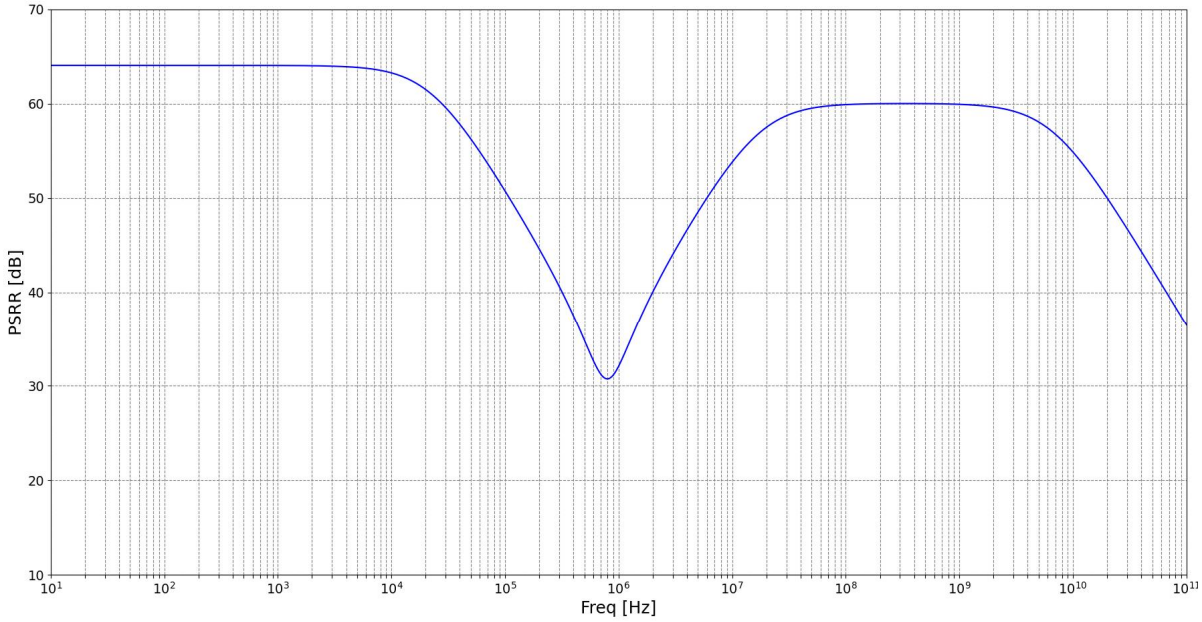

Fig. 2. Power supply rejection ratio (PSRR) for LDO

To evaluate the power supply ripple rejection (PSRR) coefficient and analyze the obtained data, a simulation of the model (a mathematical representation of the component's behavior [9]) was performed using LT Spice software.

For the PSRR measurement simulation, a power supply input source with a voltage of 1.5 V and an AC component of 200 mV (peak-to-peak) was applied, along with a load current of 10 mA. An input capacitor was not used, whereas the output capacitor had a capacitance of 0.47 μF and an equivalent series resistance (ESR) of approximately 2 m Ohm.

Fig. 2 presents the simulation results of the PSRR for the linear voltage regulator. It was established that at a frequency of 1 MHz, the PSRR value is approximately 30 dB.

The use of Lead compensation in the LDO circuit improves the PSRR by reducing phase shifts at high frequencies, which leads to effective attenuation of high-frequency noise (fluctuations). Increasing the capacitance of the capacitor C_{LEAD} in the feedback loop helps to enhance the efficiency of Lead compensation.

Fig. 3 demonstrates the effect of compensation on PSRR: as the C_{LEAD} capacitance of the capacitor increases, the circuit's ability to suppress high-frequency disturbances improves, which positively affects the PSRR.

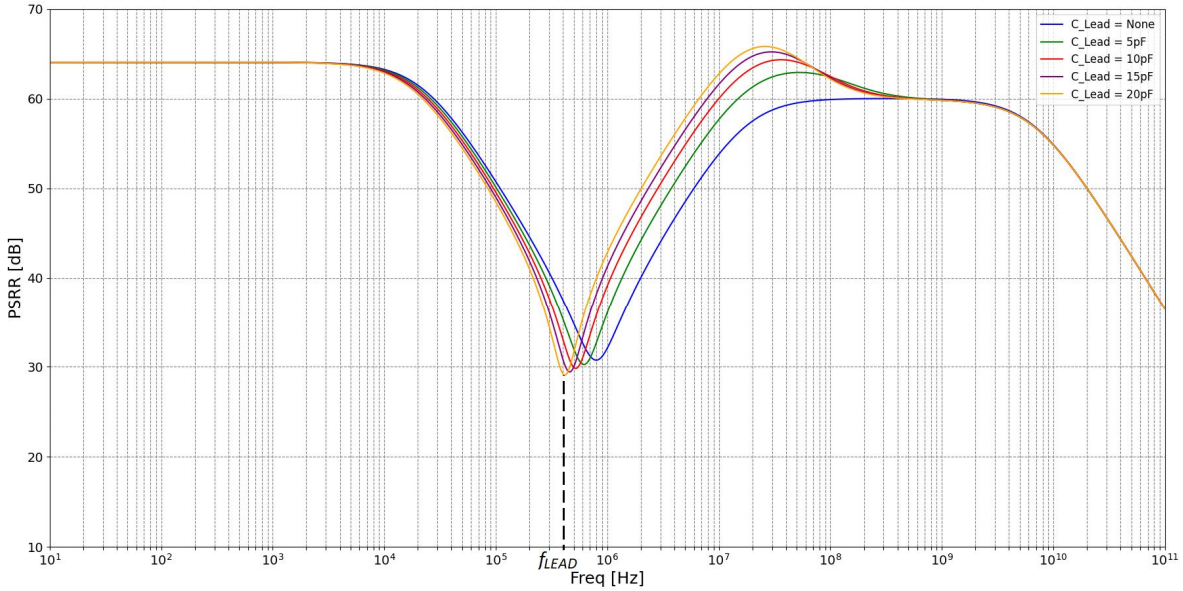

Fig. 3. Power supply rejection ratio (PSRR) for various capacitor (C_{LEAD}) values in LDO

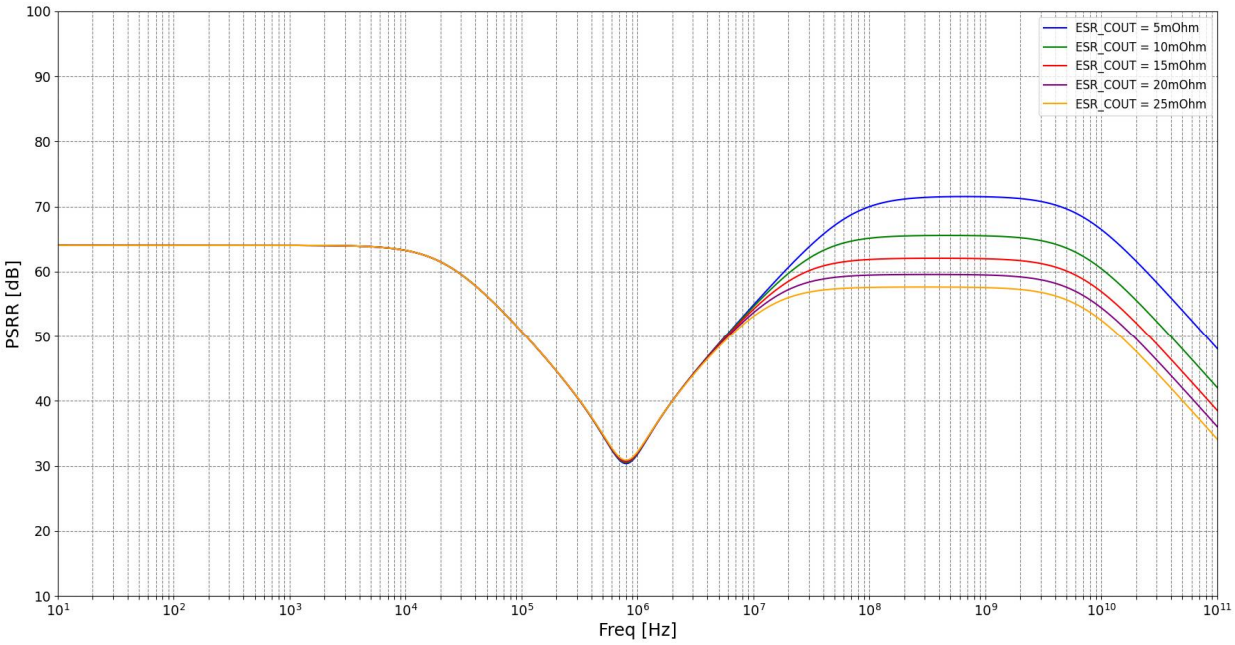

Fig. 4. Power supply rejection ratio (PSRR) for various ESR resistance values of output capacitor

The capacitance of the capacitor C_{LEAD} influences the frequency characteristics of the system, specifically, an increase in the capacitance of C_{LEAD} results in a decrease in the frequency f_{LEAD} (Fig. 3).

The resistance value of R_{LEAD} remains constant at 300 ohm. This means that the compensation effect (reduction of phase shifts) will begin to act at a lower frequency.

As C_{LEAD} increases, the phase shift φ_{LEAD} at a fixed frequency decreases, as the product of ωR_{LEAD} C_{LEAD} becomes larger. The gain at lower frequencies remains unchanged, but the gain rise region also extends to lower frequencies, and the gain in the mid-frequency range increases.

The equivalent series resistance (ESR) of the output capacitor C_{LOAD} also significantly affects the PSRR value in the LDO circuit. A large ESR value limits the ability of the output capacitor to effectively filter high-frequency disturbances due to additional energy losses in the resistive ESR component, which reduces the overall ripple rejection coefficient. Furthermore, ESR affects the

feedback characteristics of the circuit, altering the phase and amplitude margins, which can impact the dynamic stability of the LDO.

Fig. 4 presents the obtained results for PSRR at different ESR values of the output capacitor C_{LOAD}. At low frequencies, the influence of ESR is generally negligible, as the capacitance of the capacitor plays the primary role in filtering. However, at high frequencies, the filtering efficiency significantly decreases due to the increasing influence of the ESR resistance, which manifests as a deterioration in PSRR.

Fig. 4 demonstrates a decrease in the suppression coefficient at high frequencies as ESR increases. Therefore, the use of capacitors with a low ESR value is crucial for ensuring high efficiency in the operation of the LDO. However, it should be noted that the influence of ESR can vary in different applications, which is determined by the location of the dominant poles, in turn defined by the parameters of the error amplifier and RE transistor.

5. Conclusions

The Power Supply Rejection Ratio (PSRR) is a critically important parameter for ensuring the stable operation of high-performance sensors. These devices often operate with very weak signals, which can easily be distorted due to fluctuations or ripple in the power supply. A high PSRR value allows the LDO to effectively suppress these disturbances, minimizing their impact on the output voltage. This is especially important for precise measurements, such as in medical, aerospace, or analytical applications, where even minor fluctuations in the power supply voltage can lead to significant errors in data.

1. The use of Lead compensation is an important stabilization mechanism that ensures the stability of the closed-loop system in the LDO regulator. It compensates for phase shifts and improves the dynamic characteristics of the circuit, reducing the likelihood of oscillations even under unfavorable load conditions. For the LDO, the presence of properly tuned Lead compensation guarantees stability and minimal fluctuations in the output voltage, which is particularly important for sensors with high sensitivity to changes in power supply parameters.

2. The output capacitor C_{LOAD} is an important stabilization element in the LDO circuit, as it determines the level of fluctuations and oscillations in the output voltage. A low value of the equivalent series resistance (ESR) of the capacitor allows for more effective filtering of high-frequency oscillations, improving the quality of the output signal. Incorrect selection of the capacitor can lead to degradation of the stability and accuracy of the regulator, so careful attention to selecting this component is required during the circuit design process.

Conflict of Interest

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