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RESEARCH AND DESIGN OF A MATRIX MULTIPLIER ON FPGA

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***Abstract*: This paper presents a comprehensive investigation and hardware implementation of a multi-bit Brawn matrix multiplier architecture. The research focuses on analyzing the system characteristics of binary multipliers realized with both conventional and optimized full and half adders. Particular attention has been given to the applicability of such multipliers within arithmetic logic units (ALUs) for vector and scalar processing architectures. Analytical models have been formulated to quantify hardware resource utilization and computational latency across various logic base configurations. The proposed multiplier has been described using the VHDL hardware description language and validated through functional simulation. The designs have been synthesized and implemented on Xilinx FPGA platforms. It has been established that the use of improved full and partial binary adders as part of the Brown matrix multiplier reduces the hardware complexity by a factor of 1.7 and increases the performance by a factor of 2.9 compared to the known classical structures of binary adders. The use of multibit Brown matrix multipliers with an improved element base allows to significantly speed up the execution time of the multiplication operation of special-purpose processors and vector and scalar supercomputers.**

***Index terms*: matrix multiplier, half and full adder, ALU, FPGA, synthesis, topology.**

I. INTRODUCTION

Binary multiplication is a fundamental operation widely employed in cryptanalysis tasks, digital image and signal processing, RGB pixel transformations, and spectral analysis. This operation is typically implemented using either software-based or hardware-based techniques [1–3].

Multi-bit binary multipliers are extensively utilized in coprocessors, processor control units, arithmetic logic units (ALUs), specialized signal and image processing processors, as well as in both vector and scalar processing architectures [1–5].

Functionally and structurally, multiplication can be performed using software methods that rely on sequential algorithms or other approaches based on analytical expressions [3, 4, 6]. Alternatively, hardware-based implementations offer another approach, including parallel, sequential, and hybrid parallel-sequential architectures [3–6].

One of the primary indicators of efficiency in multibit matrix and tree-structured multipliers is their ability to maintain high computational throughput, which is largely determined by the minimization of signal propagation delays during the formation of partial sums and the transmission of carries within the underlying single-bit binary adder cells.

Additional essential performance metrics include minimal structural complexity in reduced input/output overhead and low hardware complexity.

A wide array of architectural implementations exists for single-bit half binary adders and full binary adders, many of which are integral building blocks in the design of matrix and multilayer binary multipliers.

Accordingly, the development of multi-bit matrix multipliers utilizing optimized single-bit adder cells, along with a comprehensive evaluation of their system-level performance characteristics, represents a timely and practically important direction of research.

II. LITERATURE REVIEW AND PROBLEM STATEMENT

Arithmetic operations encompass addition, subtraction, multiplication, division, comparison, and square root extraction [1, 3, 5, 6].

Among these, multiplication is the second most frequently performed operation in computational systems, following addition. Several methods exist for accelerating multiplication, such as altering the encoding of the operands to reduce the number of partial products (Booth's algorithm) [7], utilizing more efficient summation techniques for partial products that minimize the time spent on carry propagation, and implementing parallel computation of all partial products [2, 3]. These approaches are typically realized using combinational logic circuits.

Parallel computation of partial products is a fundamental aspect of all multiplication schemes. The primary distinction between different architectures lies in the method of summing the partial products. Based on this, multipliers can be categorized into matrix-based and multi-layer tree-structured designs. The difference between these types is expressed in the number of single-bit adders utilized, their configuration, and the technique employed for carry propagation during summation.

In matrix multipliers, summation is performed by a matrix of adders, which consists of sequential rows of single-bit adders with carry propagation. As the data progresses downward through the array of adders, each row of the carry-save adders adds the next partial product to the accumulated sum of partial products. Matrix multipliers achieve high performance and exhibit a significant degree of regularity, which is particularly advantageous when implementing such multipliers as integrated circuits. On the other hand, such circuits occupy a large area on the chip, and with the increase in the bit depth of the multipliers, this area increases in proportion to the square of the number of bits. Another disadvantage of matrix multiplier is its low hardware utilization. As the sum of partial products propagates down the matrix, each row is used only once when it intersects with the active computation phase. This characteristic can be exploited to enhance computational efficiency by pipeline processing, where, as each row is freed up, it can be reused to multiply the next pair of operands.

Some of the most well-known matrix multipliers include the Brown multiplier, the carry-propagating multiplier [5, 9], as well as multipliers based on the Boole-Vulli [3, 4] and Pezaris [3] algorithms, designed for multiplication of binary numbers in two's complement representation.

To reduce the delay typical of matrix multipliers, designs based on tree-like structures can be utilized. While multi-layer multipliers exhibit faster performance than matrix-based structures, their implementation requires additional connections to merge bits of the same weight. This can result in a larger chip area than in matrix-based adder configurations.

In multi-layer multipliers, summation is achieved through a tree-like structure, primarily focusing on the compression of partial products with the same weight by employing single-bit full adders (3–2) and half adders (2–2). Known single-bit adders with input-output ratios such as (5–3), (7–3), (15–4), and others are referred to as counters. This is because the output code of these adders, similar to that of a binary counter, corresponds to the number of units at the inputs [2–5].

Among the most widely used multi-layer multipliers are tree-based schemes implemented using the Wallace [9, 10] and Dadda [11, 12] algorithms.

III. SCOPE OF WORK AND OBJECTIVES

The development of high-performance specialized computing systems is an urgent task in the current conditions of dynamic growth in demand for high-speed multi-bit components of ALUs vector and scalar processors used in the field of artificial intelligence (AI). At the same time, an important task is to investigate the system characteristics of high-speed multi-bit matrix multipliers based on improved structures of half adders and full adders [1–6].

The main goal of the work is to study and design multi-bit high-speed matrix multipliers on FPGAs for their further use in signal and image processing systems, cyber-physical systems, and tasks of processing RGB pixels of color images [4–6].

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IV. DESIGN OF THE ARCHITECTURE OF THE BRAWN'S MATRIX MULTIPLIER

Fig. 1 shows the structure of a 4×4 Braun matrix multiplier. This architecture incorporates single-bit binary half adders (HA) and full adders (FA) [2–6].

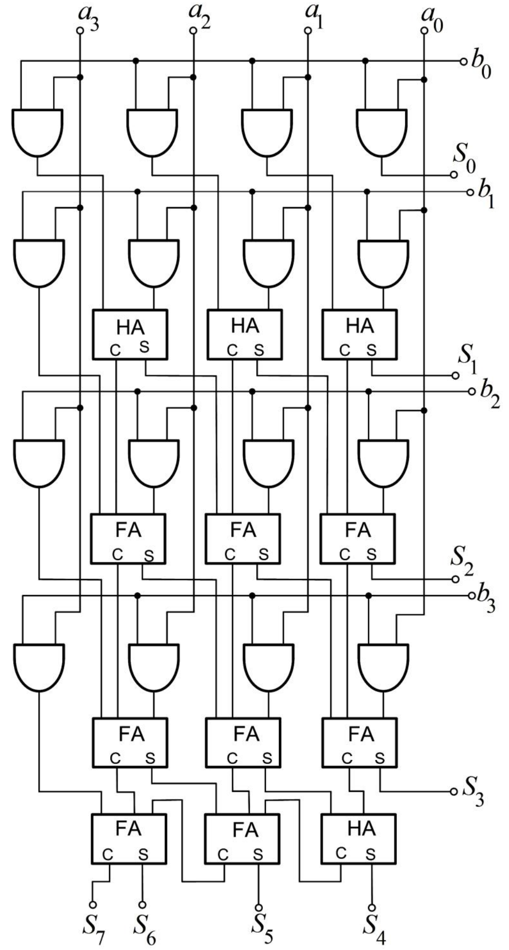


Fig. 1. Structure of the Brown 4×4 matrix multiplier

The overall hardware complexity of the Braun matrix multiplier can be estimated using the following expression:

$$A_{MM} = (n^2 \times A_{LE}) + (n \times A_{HA}) + (n^2 - 2n) \times A_{FA}, \quad (1)$$

where n – bit-length of the input data; A_{LE} – hardware complexity of logical element "AND"; A_{HA} – hardware complexity of a HA; A_{FA} – hardware complexity of a FA.

Let's calculate the hardware complexity of a matrix multiplier based on the well-known classical full adders and half adders [3], the structures of which are shown in Fig. 2.

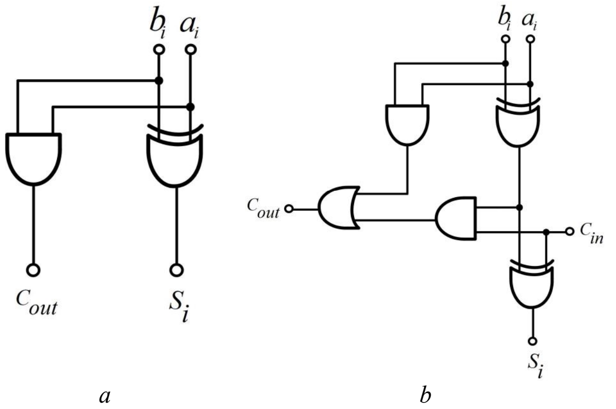


Fig. 2. Structure of a classical half adder (a) and full adder (b)

The hardware complexity of a binary half adder is represented by 5 logic gates, with a time complexity of 3 clock cycles for the sum signal generation and 1 microcycle for the carry signal generation.

The hardware complexity of a full binary adder is composed of 11 logic gates, with a time complexity of 6 microcycles for sum signal generation and 5 microcycles for carry signal generation.

For example, with $n = 4$ using classical full and half adders, the hardware complexity of the Brown matrix multiplier is calculated as follows:

$A_{MM1} = (4^2 \times 1) + (4 \times 5) + (4^2 - 8) \times 11 = 124\,(gate)$.

In [13], an improved structure of a half binary adder was proposed, which is shown in Fig. 3.

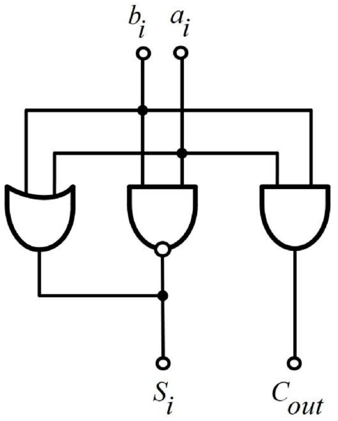


Fig. 3. Structure of an improved half adder

The hardware complexity of the improved binary half adder is 3 gates, and its time complexity is 1 microcycle when generating the sum and carry-out signals.

An improved structure of a full binary adder is proposed in [14], which is shown in Fig. 4. The hardware complexity of the improved full binary adder is comprised of 6 logic gates, while its time complexity is 2 microcycles for the generation of the sum and carry-out signals.

For example, with $n = 4$ the use of the improved HA and FA, the hardware complexity of a matrix multiplier is as follows:

$$A_{MM2} = (4^2 \times 1) + (4 \times 3) + (4^2 - 8) \times 6 = 76\,(gate).$$

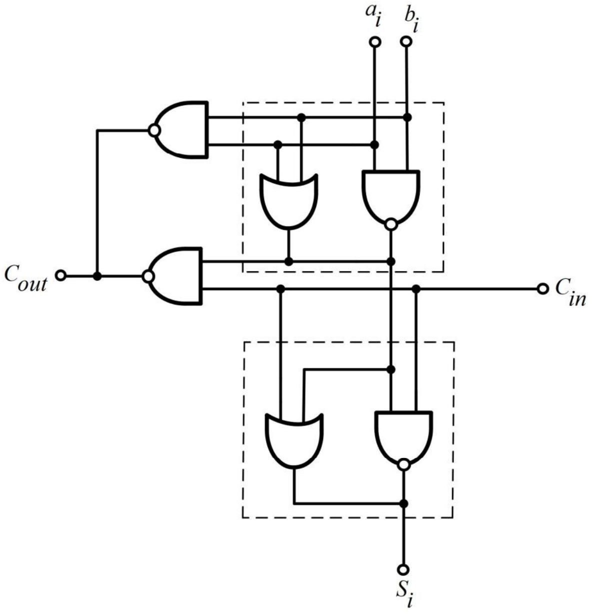


Fig. 4. Structure of an improved full adder

That is, the hardware complexity of the Brown matrix multiplier will be 1.7 times less with the use of improved HA and FA.

Table 1 shows the obtained values of the hardware complexity of multi-bit Brown's matrix multipliers based on classical and improved HA and FA

Table 1

The hardware complexity of Brown's matrix multipliers

Brown's matrix multiplier bit-length	Number of gates when using classic HA and FA (A_{MM1})	Number of gates when using advanced HA and FA (A_{MM2})
8	624	372
16	2784	1648
32	11712	6880
64	48000	28096
128	194304	113536
256	781824	456448
512	3136512	1830400

Based on the values of hardware complexity obtained in Table 2, we see that the hardware complexity of a multibit matrix multiplier (n = 512) is 393984 gates when using improved NS and PS.

The time complexity of the Brown matrix multiplier is calculated according to the following formula:

$$t_{MM} = t_{LE} + (2 \times t_{HA}) + (2n - 4) \times t_{FA}, \qquad (2)$$

where n – bit-length of the input data; t_{LE} – time complexity of logical element "AND"; t_{HA} – time complexity of a HA; t_{FA} – time complexity of a FA.

For example, with $n = 4$ the use of the improved HA and FA, the time complexity of a matrix multiplier is as follows: $t_{MM1} = 1 + (2 \times 3) + (8 - 4) \times 6 = 31\,(microcycle)$.

When using improved HA and FA, the time complexity of the Brown matrix multiplier will be: $t_{MM2} = 1 + (2\times1) + (8-4)\times2 = 11(microcycle)$.

That is, the time complexity of the 4×4 matrix multiplier will be 2.9 times less with the use of improved HA and FA.

Table 2 shows the obtained values of the time complexity of multibit Brown's matrix multipliers based on classical and improved HA and FA.

Table 2

The time complexity of Brown's matrix multipliers

Brown's matrix multiplier bit-length	Time complexity when using classic HA and FA (t_{MM1})	Time complexity when using advanced HA and FA (t_{MM2})
8	79	27
16	175	49
32	367	123
64	751	249
128	1519	507
256	3115	1039
512	6127	2043

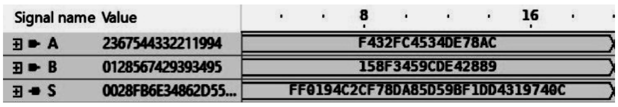
Based on the values of the time complexity obtained in Table 2, we see that the time complexity of the multi-bit matrix multiplier (n = 512) is 2043 microcycle when using improved HA and FA.

V. MODELLING AND SYNTHESIS OF BROWN'S MATRIX MULTIPLIER ON FPGA

The development of multi-bit Brown multipliers was carried out using the Verilog hardware description language within the Active HDL SE integrated environment [15].

Fig. 12 shows a diagram of the functional simulation of the 64×64 Brown matrix multiplier.

This diagram shows the transmission of 128-bit integer binary values to the inputs of *A* and *B*. The output *S* is the 128-bit result of the product of the input data.



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Signal name Value                          8               16
A           2367544332211994   F432FC4534DE78AC
B           0128567429393495   158F3459CDE42889
S           0028FB6E34862D55...  FF0194C2CF78DA85D59BF1DD4319740C
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Fig. 5. Functional diagram of the 64-bit Brown matrix multiplier

The synthesis of the 64-bit Brown matrix multiplier was performed on the Artix-7 FPGA family, specifically the XC7A100TCSG324-1 chip from Xilinx.

In an enlarged view, Fig. 5 represents a section of the FPGA crystal on which the structure of the 64-bit Brown matrix multiplier was implemented in the Vivado Design Suite CAD software.

As a result of the synthesis and implementation of a 64-bit Brown matrix multiplier based on improved HA and FA on the selected FPGA chip, the following hardware costs were obtained. In total, the implementation of such an MPB requires 376 LUTs out of the available 63400 on the FPGA chip.

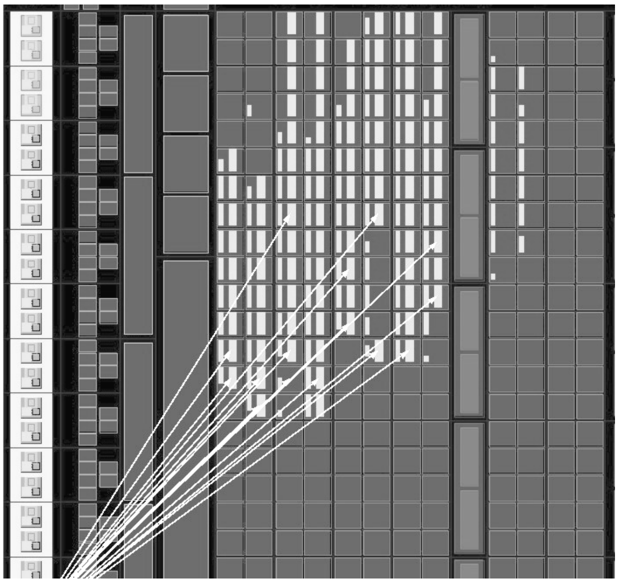

Fig. 6. Implementation of a 64-bit Brown matrix multiplier on a FPGA chip in Vivado CAD

Table 5 shows the results of synthesizing a 64-bit Brown matrix multiplier on an Artix-7 FPGA using classical and advanced components of single-bit HA and FA.

Table 3

Results of synthesis of a 64-bit Brown matrix multiplier on FPGA

System characteristics	Brown's matrix multiplier is based on classical HA and FA	Brown's matrix multiplier is based on advanced HA and FA
Hardware cost (Number of LUTs)	674	376
Performance (Frequency, MHz)	132	365

From the results shown in Table 3, we can see that the hardware costs for implementing a 64-bit Brown matrix multiplier based on advanced HA and FA are about 1.8 times less than the cost of implementing such a multiplier on classical HA and FA, and the speed is about 2.8 times faster.

VI. CONCLUSION

In this paper, a matrix multiplier of Brown's binary numbers was developed, which is a component of arithmetic and logic devices of vector and scalar processors. A review of hardware methods of binary number multiplication was carried out and it was determined that matrix and tree multipliers have high speed of implementation of this operation. The system characteristics of the implementation of such multipliers on classical and advanced components of half and full binary adders were analyzed. The design and modeling of a 64-bit Brown matrix multiplier using the VHDL hardware description language were considered. When synthesizing such a multiplier on FPGAs in Vivado CAD, a 1.8-fold reduction in hardware complexity and a 2.8-fold increase in performance were obtained compared to the use of the classical element base of HA and FA, which was confirmed by theoretical calculations.

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