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DEVELOPMENT OF I²C LEVEL SHIFTER USING μASIC

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Abstract: This paper presents the design and implementation of an I²C level shifter using the AM1U1420 single-chip solution. The device enables seamless voltage translation between different I²C logic levels, ensuring reliable communication between components operating at varying supply voltages. The AM1U1420 can integrate bidirectional level shifting functionality, reducing the need for external components and simplifying circuit design. We analyze its electrical characteristics, performance metrics, and practical application scenarios. Experimental results confirm the chip's efficiency in maintaining signal integrity and low propagation delay. This solution is particularly beneficial for modern embedded systems, IoT devices, and mixed-voltage environments.

Key words: I²C, level shifter, power consumption, clock, CMOS, μASIC, IoT device.

1. Introduction

The I²C (Inter-Integrated Circuit) bus is widely used for communication between low-speed peripheral devices in embedded systems, sensors, and microcontrollers. However, as modern electronics increasingly incorporate components operating at different voltage levels, reliable voltage translation is essential to ensure proper communication. Traditional level-shifting solutions often require multiple discrete components, increasing circuit complexity and board space.

The AM1U1420 can be used as single-chip level shifter and provide an efficient and compact solution for bidirectional voltage translation in I²C applications. It enables seamless communication between devices operating at different voltage domains, reducing design complexity and improving system reliability. This paper explores the functionality, implementation, and performance of the AM1U1420, demonstrating its advantages over conventional level-shifting methods. Experimental results validate their effectiveness in maintaining signal integrity and low propagation delay, making it an ideal choice for embedded systems, IoT applications, and mixed-voltage environments.

Level shifting for I²C communication has been extensively studied, with various approaches proposed to ensure compatibility between devices operating at different voltage levels. Traditional solutions often rely on external pull-up resistors and MOSFET-based circuits to achieve bidirectional voltage translation. For example, the classic BSS138-based level shifter is widely used due to its simplicity and low cost. However, such discrete implementations can introduce signal degradation, increased propagation delay, and the need for careful resistor selection to balance speed and power consumption [1].

Several dedicated level-shifting ICs, such as the PCA9306 [2] and TXB0108 [3], have been developed to address these challenges, offering integrated solutions for I²C and other low-speed digital interfaces. These ICs improve performance by incorporating built-in pull-ups, low on-resistance, and adaptive drive strength. However, many existing solutions still require external components, occupy significant board space, or lack optimized power efficiency for modern applications.

The AM1U1420 represents a more advanced alternative by integrating bidirectional I²C level shifting into a single compact package. Unlike traditional solutions, it minimizes external component requirements while maintaining high signal integrity and low power consumption. This paper builds upon previous work by evaluating the AM1U1420's performance in real-world applications, comparing it with existing methods, and highlighting its advantages in embedded system design.

The I²C bus is a widely used for short-distance communication between integrated circuits. Developed by Philips (now NXP Semiconductors), I²C enables multiple devices, such as microcontrollers, sensors, memory chips, and displays, to communicate using only two signal lines: SDA (Serial Data Line) and SCL (Serial Clock Line). This simplicity makes it ideal for embedded systems, IoT devices, and consumer electronics.

I²C operates on a master-slave architecture, where one or more master devices control communication with multiple slaves. The bus supports multiple data rates, including Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1 Mbps), and High-Speed Mode (3.4 Mbps) [5]. Each device on the bus is assigned a unique address, allowing efficient data exchange using a defined protocol.

A key feature of I²C is its open-drain design, where pull-up resistors are required to maintain proper voltage levels. This design enables multiple devices to share the

same bus while avoiding signal contention. However, when devices operate at different voltage levels (e. g., 1.8 V and 3.3 V), voltage level shifting is necessary to ensure reliable communication.

To address this challenge, various level-shifting techniques have been developed, ranging from simple MOSFET-based circuits to dedicated level-shifter ICs. The AM1U1420, discussed in this paper, offers an integrated, efficient solution for bidirectional I²C voltage translation, simplifying design and enhancing system reliability.

The µASIC family consists of programmable ultra-small mixed-signal ICs that include logic macrocells, I²C interface, oscillators, ACMPs, a temperature sensor, a voltage reference (VREF), and other features.

In this study, we used the AM1U1420, an ultra-small programmable µASIC. Each macrocell within the AM1U1420 offers multiple configurable settings and initial states, providing maximum flexibility for various applications. Main features [6]:

- 1.71 V to 5.5 V supply (V_{DD}).
- 1.10 V to V_{DD} (V_{DD2}).
- Operating temperature range: –40 ºC to 85 ºC.
- RoHS compliant/Halogen-free/Pb-free.
- Contains 4 analog comparators (ACMP).
- Has voltage reference (V_{REF}).
- Temperature sensor (*TS*).
- I²C Protocol compliant
- Twenty-seven multifunctional macrocells.
- Two oscillators.
- Power on reset.
- Data protection features:
  - CRC-8;
  - Continuous register verification.

2. Experimental part

2.1. Implementation of I²C level shifter on AM1U1420

The I²C level shifter on the µASIC utilizes a single IC-AM1U1420-along with four resistors that pull up the PMOS output to the voltage source. Adjusting the resistance of these resistors impacts power consumption and the strength of the pull-up.

The I²C interface relies solely on an open-drain NMOS output. Since both SDA and SCL are bidirectional, both the master and slave can pull the signals LOW.

The µASIC was configured by using Atlas EDA.

The examples of I²C level shifter schematics and its design configuration are presented in Fig. 1 and Fig. 2. This configuration is designed exclusively for I²C, utilizing an open-drain NMOS output. The oscillator (OSC1) is set to auto mode, meaning it activates only when a signal is present. Each level shifter channel automatically detects the direction of communication by sensing which line is pulled LOW first. Upon power-up, all I/O pins default to input mode, waiting for a signal. After the signal transition, the I/O pins remain in input mode, awaiting further signals. Additionally, there is an option to disable outputs via IO2 or through an I²C command.

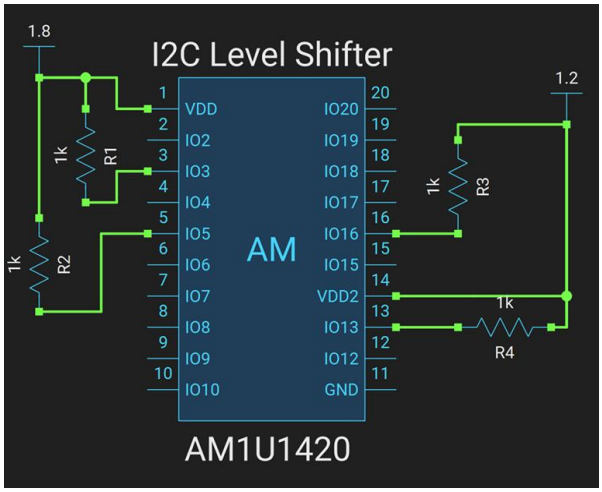

Fig. 1. I²C level shifter schematic example.

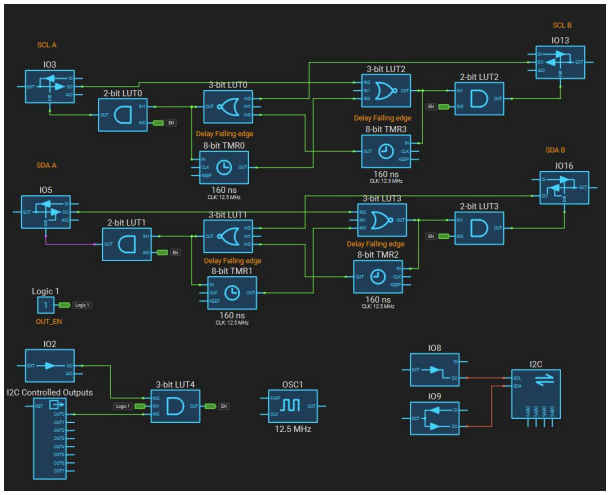

Fig. 2. I²C level shifter design.

The experimets were carried out with next the following conditions:

- Temperature: room temperature (25 ºC).
- V_{DD} = 1.8 V.
- V_{DD2} = 1.2 V.
- Scope probe capacitance: 11 pF.
- Scope input capacitance: 17 pF.
- Channel 1 (yellow) – I²C SDA A 1.8V (IO5).
- Channel 2 (blue) – I²C SCL A 1.8V (IO3).
- Channel 3 (magenta) – I²C SDA B 1.2V (IO16).
- Channel 4 (green) – I²C SDA A 1.2V (IO13).

In Figs. 3–5 we see the output test of the device.

Fig. 3. I²C Level shifter scope shot, 3.4 MHz frequency (A to B transition).

Fig. 4. I²C Level shifter scope shot, 3.4 MHz frequency (B to A transition).

Fig. 5. I²C Level shifter scope shot, 3.4 MHz frequency (outputs disable).

3. Analysis of current consumption

In Quiescence, the chip consumes a small amount of current (Fig. 6).

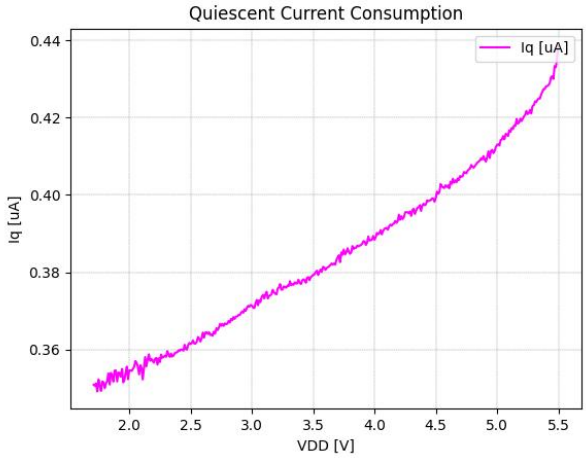

Fig. 6. Quiescent current consumption.

The results of Fig. 6 are summarized in Table 1.

Table 1

Quiescence current consumption

V_{DD}, V	I_q, µA
1.71	0.350
1.8	0.351
3.3	0.376
5.0	0.413
5.5	0.438

The µASIC consumes an ultra-low amount of power, with its internal oscillators being the primary contributors to power consumption. To minimize this, it is crucial to stop OSC1 when no signal is present. Auto mode handles this by putting the oscillator into an IDLE state when there is no signal on the timers or any signal forcing activation. In this state, power consumption is significantly reduced to just 250 nA at V_{DD} = 3.3 V.

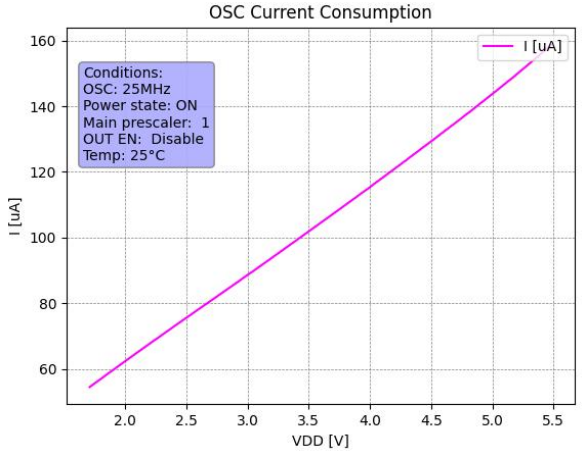

Fig. 7. OSC1 current consumption ON state.

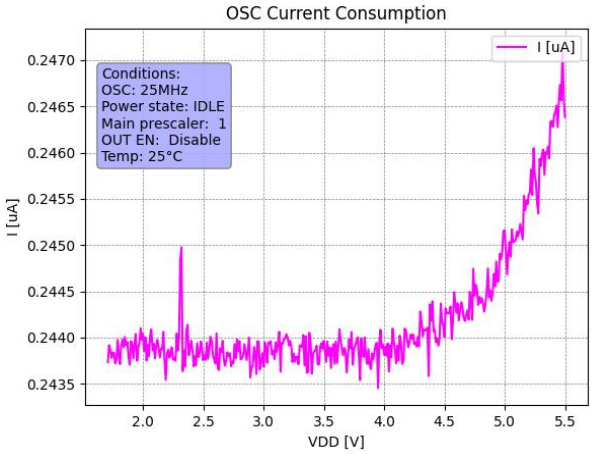

Fig. 8. OSC1 current consumption IDLE state.

The results of the oscillator current consumption are summarized in Table 2. As it follows, when sending packages, current consumption rises. It also depends on operating voltages. The higher V_{DD} – the higher current consumption (Figs. 7, 8).

Table 2

Current consumption of oscillator

OSC Mode	Power supply range V_{DD}					Unit
	1.71 V	1.8 V	3.3 V	5.0 V	5.5 V	
IDLE	0.24	0.24	0.24	0.25	0.25	µA
ON	44.97	46.93	77.26	113.37	125.39	µA

4. Conclusion

The experiment demonstrated that a Bidirectional I²C level shifter can be successfully implemented using the AM1U1420 chip. This chip has a low quiescent current consumption of 0.35 µA, which increases up to 125.39 µA during data transmission. A minor measurement error occurred due to the capacitance of the oscilloscope. All experiments were conducted at room temperature. The output signal exhibited a delay of one clock cycle.

To handle Standard mode, Fast mode, Fast mode plus, High-speed mode (1.7 Mbit/s) 2 MHz oscillator can be used. This will reduce the current consumption significantly.

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РОЗРОБЛЕННЯ I²C ПРИСТРОЮ ЗСУВУ РІВНЯ З ВИКОРИСТАННЯМ μASIC

Данило Таланчук, Віталій Риботицький,
Степан Нічкало, Анатолій Дружинін

У статті наведено дизайн і реалізацію пристрою зсуву рівня I²C із використанням однокристального рішення AM1U1420. Пристрій забезпечує плавний перехід напруги між різними рівнями логіки I²C, а також надійний зв'язок між компонентами, що працюють за змінних напруг живлення. AM1U1420 може інтегрувати функцію двонаправленого зсуву рівня, зменшуючи потребу в зовнішніх компонентах і спрощуючи дизайн схеми. Проаналізовано електричні характеристики, показники продуктивності та потенційне практичне застосування пристрою. Експериментальні результати підтверджують ефективність мікросхеми у збереженні цілісності сигналу та низької затримки поширення. Це рішення особливо корисне для сучасних вбудованих систем, пристроїв інтернету речей і пристроїв, що оперують за комбінованих напруг.

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