ІНФОКОМУНІКАЦІЙНІ ТЕХНОЛОГІЇ ТА ЕЛЕКТРОННА ІНЖЕНЕРІЯ
INFORMATION AND COMMUNICATION TECHNOLOGIES, ELECTRONIC ENGINEERING

№ 5 (2), 2025

РАДІОЕЛЕКТРОНІКА

https://doi.org/10.23939/ictee2025.02.

POWER LINE COMMUNICATION SYSTEM WITH NFC CONTROL FOR IOT DEVICES

L. Tarasenko [ORCID: 0009-0008-2869-1436]

Lviv Polytechnic National University, 12, S. Bandery str., Lviv, 79013, Ukraine

Corresponding author: L. Tarasenko (e-mail: lev.o.tarasenko@lpnu.ua).

(Received 7 June 2025)

Power Line Communication is a technology that enables the transmission of data signals over existing power lines, allowing electrical wiring to serve a dual purpose: delivering power and enabling data communication. It is widely used in both residential and industrial settings to create communication networks without the need for additional dedicated wiring. Proposed technology can be a highly effective for the systems with limited physical access, or even for the already built systems modernization. This paper describes the modified physical layer inside of the PLC networks. This type of communication intended to work for DC power nodes. The data transmission takes place between PLC host and PLC nodes. Each step of the signal transfer is validated on the laboratory bench setup with signal quality calculations. Bench measurements are followed by a software simulation. The PLC Host receives transmission data from NFC EEPROM and performs signal procession then, forms analog waveform for injection. The paper contains a detailed NFC-V protocol analysis and description with communication waveform sample capturing and decoding operations. As the result of signal procession, the main PLC controller block forms a certain sequential analog signal, that is injected into feedback of the DC-to-DC converter. The PLC controller output signal described as a custom physical layer for proposed communication protocol. The PLC node, connected to a powerline, powered by the PLC Host. The node uses only the negative and positive power rails as the signals for both data transfer and self-powering functions. The received modulated signal passes through a band pass filter with 15 kHz centre frequency, 158 MHz bandwidth and amplification stage of 20 dB. The analog to digital decode operations are handed by a mixed signal ASIC. The decode results are validated on laboratory bench setup with visual ASK to SPI decode operation representations. The modulation signal, injected into the power line, is compared with return signal, received from power node after the filtering and amplification stages. Paper contains a resulting quality parameter analysis and system feasibility conclusions.

Keywords: *PLC, DC-DC, ASK, Feedback, THD, SNR, NFC.*
УДК: 621.39

Introduction

The PLC Network [1] consist of three basic components: PLC Host, power line and PLC nodes. The PLC Host is a central node that initiates communication and sends or receives data and injects modulated data signals onto the power line. Power Line acts as a shared transmission path for both power and data. PLC Nodes – end devices such as smart meters, sensors, or appliances. They receive and decode the data;

some nodes may respond or retransmit data. This diagram in Fig. 1 illustrates the architecture of a Power Line Communication (PLC) system used for both power delivery and data transmission across multiple nodes. At the beginning of the setup, power input (PWR IN) is supplied to a central PLC Host. This host device serves as the main controller and initiator of communication within the network. It injects both power and data signals into the system through the shared Power Line. From the PLC Host, the power line continues and distributes both electrical power and communication signals downstream.

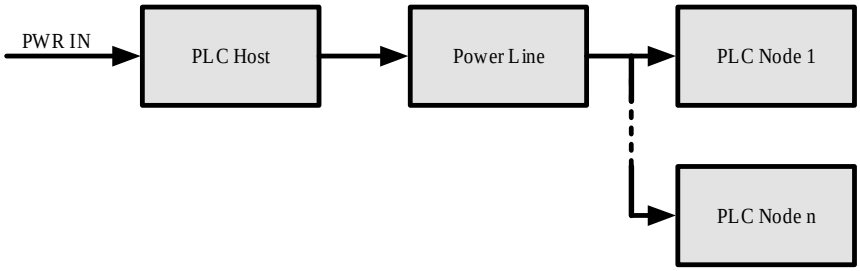

Fig. 1. PLC system general diagram

Multiple PLC Nodes are connected along the power line – labelled as PLC Node 1, PLC Node 2, and so on, up to PLC Node n. These nodes act as receivers or endpoints in the communication network. Each one can interpret the signals sent by the host and, depending on the protocol, may also send data back. The topology shown is a bus configuration, where all nodes share the same power and communication line. This is a common layout in industrial and smart energy applications because it reduces wiring complexity and allows for easy scaling by simply adding more nodes to the power line.

Power Line Communication (PLC) traditionally refers to the transmission of data over existing power lines, allowing devices to communicate without the need for additional wiring. While it is commonly used on AC mains infrastructure, PLC can also be implemented on DC power lines, which are increasingly prevalent in applications such as electric vehicles, industrial automation, battery management systems, and DC microgrids. In a DC PLC system, the DC power line serves a dual purpose – supplying power and acting as the communication medium. Instead of using high-frequency carriers superimposed on an AC waveform as in traditional PLC, the data signal is embedded into the voltage ripple of the DC power rail itself. This is made possible through modulation techniques applied in the feedback loop of DC-DC converters [2]. A DC Power Line Communication (PLC) system can be effectively integrated into a variety of modern electronic and power infrastructures. In Battery Management Systems (BMS) [3], it enables efficient cell-level monitoring and control across series-connected battery strings without additional communication wiring. In the automotive sector, DC PLC reduces wiring complexity by allowing communication between electronic control units (ECUs), sensors, and actuators over the same lines used for power distribution. In DC microgrids and renewable energy applications, PLC facilitates data exchange between distributed power converters and central supervisory controllers, enhancing system coordination and energy efficiency. LED lighting systems benefit from simplified installation and operation by transmitting control commands through the same DC lines used to power the lights. In the healthcare industry, DC PLC can be used in medical devices and diagnostic equipment to transmit control and monitoring data over shared power lines, minimizing cable clutter, and improving safety and maintainability in sensitive clinical environments.

2. The PLC host overview

The PLC host circuit designed to perform data modulation directly on a DC power line by leveraging the feedback path of a step-down DC-DC converter. The system also integrates NFC EEPROM for wireless configuration, making it well-suited for intelligent and reprogrammable power distribution or control networks [4].

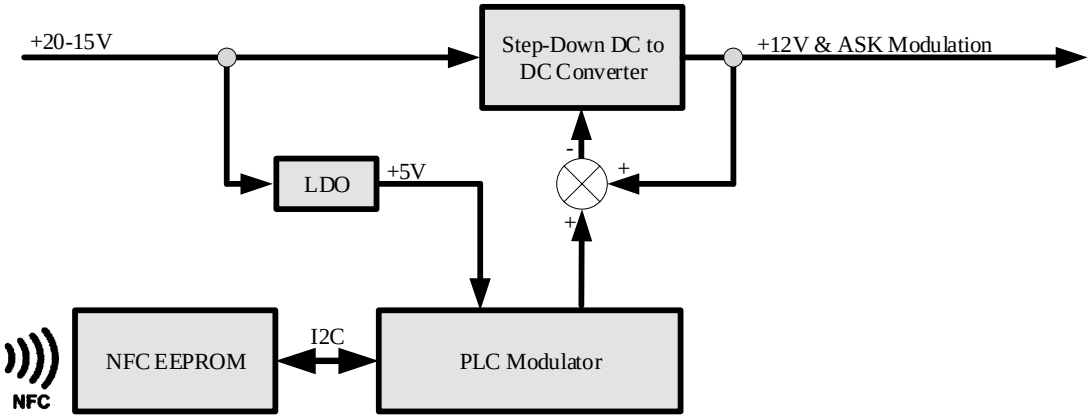

Fig. 2. PLC host block diagram

The system receives a DC input voltage in the range of +20 V to +15 V, which powers the entire PLC host. This input is routed to a step-down DC-DC converter, which generates a stable +12 V output for the power line. The core of the modulation process take place in the feedback loop of the DC-DC converter. A PLC Modulator block dynamically adjusts the feedback reference using a controlled ASK signal that encodes data. This adjustment causes subtle, controlled variations in the output voltage (ripple) of the converter, which the receiving nodes along the power line can interpret as digital data – effectively using the power line for both energy and information transfer. To supply the PLC modulator, a Low Dropout Regulator (LDO) converts the +20–15 V input rail into a stable +5 V power source. The modulator injects data into the feedback loop of a step-down DC-DC converter, which produces a +12 V output line with ASK-modulated communication signals superimposed. This modulated power line is then distributed to downstream PLC nodes, enabling both energy delivery and data transmission over a single conductor. Configuration data for the modulator is stored in an NFC EEPROM, which interfaces with the modulator via I2C and can be updated wirelessly using an NFC-enabled device, such as a smartphone.

Near Field Communication is a wireless technology that enables devices to exchange data over very short distances, usually within a few centimetres. It's commonly used for contactless payments, ticketing, access control, file sharing, and product authentication. NFC is energy-efficient, easy to use, and allows quick, secure transactions with minimal user input. Communication usually takes place between NFC readers (devices) and NFC tag [5], but also exists applications where NFC reader exchanges data with another NFC reader or NFC reader exchanges data with multiple tags at the same time.

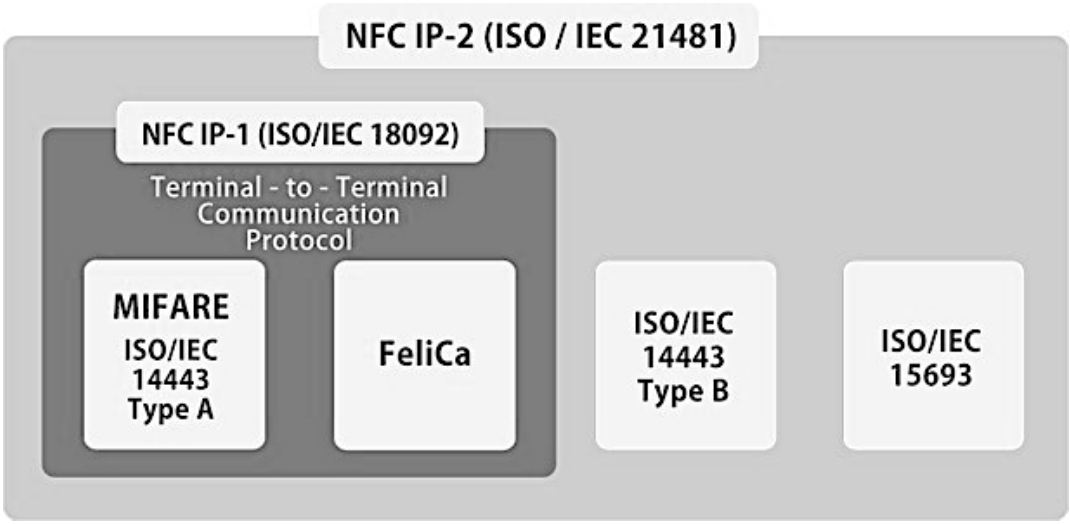

Fig. 3. NFC tag standards

The NFC tag type 1 based on NFC-A technology, simple memory structure. NFC Tag Type 1 is a low-cost, simple tag based on ISO 14443A, offering basic read / write capability at 106 kbit/s with memory typically around 96 bytes (up to 2 KB). It lacks encryption but can be permanently write-locked. Best suited for simple tasks like linking to URLs or basic identification in low-security, high-volume applications.

The NFC tag type 2 also uses NFC-A; supports NDEF and is widely adopted. One of the most noticeable technologies for type 2 is MIFARE Ultralight by NXP. NFC Tag Type 2 is a widely used, cost-effective tag based on ISO 14443A, offering 48 bytes to 2 KB of memory at 106 kbit/s. It supports NDEF formatting, basic read / write operations, and permanent locking, but lacks encryption. Ideal for apps like business cards, and product labels.

The NFC tag type 3 Utilizes NFC-F (FeliCa); offers higher data rates. NFC Tag Type 3 is a high-speed, high-capacity tag based on FeliCa (JIS X 6319-4), offering up to 1 MB of memory and speeds of 212 or 424 kbit/s. It supports NDEF and moderate security, making it ideal for transit cards and payment systems, though it's less common and more expensive than Types 1 and 2.

The NFC tag type 4 compatible with both NFC-A and NFC-B; supports ISO/IEC 14443-4. NFC Tag Type 4 supports ISO 14443A/B offers up to 32 KB memory and speeds up to 424 kbit/s, with strong security features like encryption and authentication. It's ideal for secure applications like e-Passports and payment cards but is more expensive and complex than lower tag types.

The NFC tag type 5 based on NFC-V (ISO/IEC 15693); designed for longer range applications. Type 5 uses ISO/IEC 15693 for long-range communication (up to 1 meter) and offers up to 64 KB of memory at 53 kbit/s speed. It's ideal for asset tracking and inventory management but has slower data transfer and basic security. It's less commonly supported than ISO 14443-based tags.

Table 1

General NFC tag comparison

Tag Type	Tech Base	Memory	Speed
Type 1	NFC-A	96 B to 2 KB	106 kbit/s
Type 2	NFC-A	48 B to 2 KB	106 kbit/s
Type 3	NFC-F	Up to 1 MB	424 kbit/s
Type 4	NFC-A, NFC-B	Up to 32 KB	424 kbit/s
Type 5	NFC-V	Up to 64 KB	53 kbit/s

Each tag type integrates into the NFC protocol stack at different layers, depending on its underlying technology and supported standards. For instance, Type 2 tags, based on NFC-A, interact primarily at the physical and data link layers, while Type 4 tags, supporting ISO/IEC 14443-4, have more complex interactions across all layers. Proposed PLC system includes NFC-V EEPROM, that enables long-range, contactless data transfer at 13.56 MHz with data rates up to 53 kbps. It uses passive tags with 8-byte UIDs, supports read / write and anti-collision, and is ideal for inventory and asset tracking due to its longer range and moderate speed. The ISO/IEC 15693 standard defines a set of standardized commands that a reader can send to a tag to perform operations like identifying, reading, writing, and configuring the tag.

According to ISO/IEC 15693 the transmission protocol defines the mechanism used to exchange instructions and data between the NFC reader / writer or host and the NFC tag in both directions. It is based on the concept of "NFC host talks first". This means that the device does not start transmitting unless it has received and properly decoded an instruction sent by the NFC host. The protocol is based on an exchange of a request from the host, and a response from the device. Each request and each response are contained in a frame. The frame is delimited by a Start of Frame (SOF) and End of Frame (EOF). The protocol is bit oriented. The number of bits transmitted in a frame is a multiple of eight, that is an integer number of bytes. A single-byte field is transmitted least significant bit first. A multiple-byte field is transmitted least significant byte first, and each byte is transmitted least significant bit first.

The NFC Reader request consists of an SOF, flags, a command code, parameters and data, a CRC, an EOF. In a request, the "flags" field specifies the actions to be performed by the NFC Tag and whether corresponding fields are present or not.

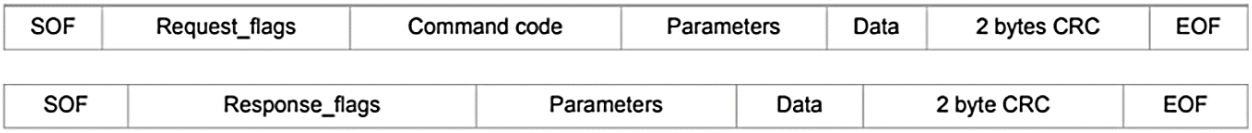

Fig. 4. NFC communication routine

The NFC tag response consists of an SOF, flags, parameters and data, a CRC, an EOF. In a response, the flags indicate how actions have been performed by the NFC Tag and whether corresponding fields are present or not. The response flags consist of eight bits.

Table 2

NFC-V Request word description

Bit	Request Flag Name	Response Flag Name
0	Sub-carrier flag	Error flag
1	Data rate flag	Extension flag
2	Inventory flag	Final response flag
3	Protocol extension flag	Extension flag
4	Select flag	Block security status length flag
5	Address flag	Block security status length flag
6	Option flag	Waiting time extension request flag
7	RFU	Reserved for future

Data coding for the host and field (NFC tag) devices are different. The host uses pulse position modulation technique, where the position determines two bits at a time. The field device uses Manchester coding for data transfer and response. The NFC tag encodes bits using Manchester coding, according to the following schemes description for the low data rate, same subcarrier frequency is used. In this case, the number of pulses is multiplied by 2 and all times increase by this factor.

Proposed PLC communication system uses "Write single block" command for EEPROM data update. The PLC transmission data byte stored in EEPROM block "0", which corresponds I2C memory address "0x00".

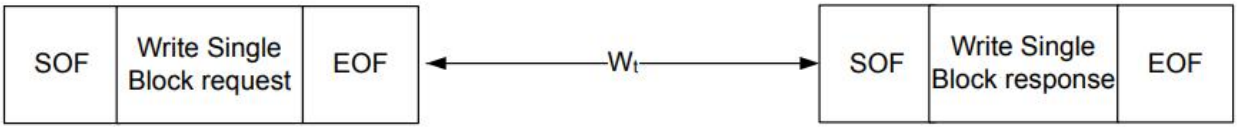

Fig. 5. Tag to host communication frame

When NFC Tag receives "Write single block" command, the device writes the data contained in the request to the targeted block and reports whether the write operation was successful in the response. When the Option flag is set, the device waits for an isolated EOF to respond. The Inventory flag must be set to 0. During the RF write cycle, there must be no modulation, otherwise the device may not correctly program the data into the memory.

Request SOF	Request_flags	Write Single Block	UID	Block number	Data	CRC16	Request EOF
-	8 bits	21h	64 bits	8 bits	32 bits	16 bits	-

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Fig. 6. "Write single block" command implementation

An NFC communication demonstration was provided using a smartphone and an ISO 15693-compliant RFID tag. EMI [6] probe and digital oscilloscope used to capture and analyse the transmitted signals.

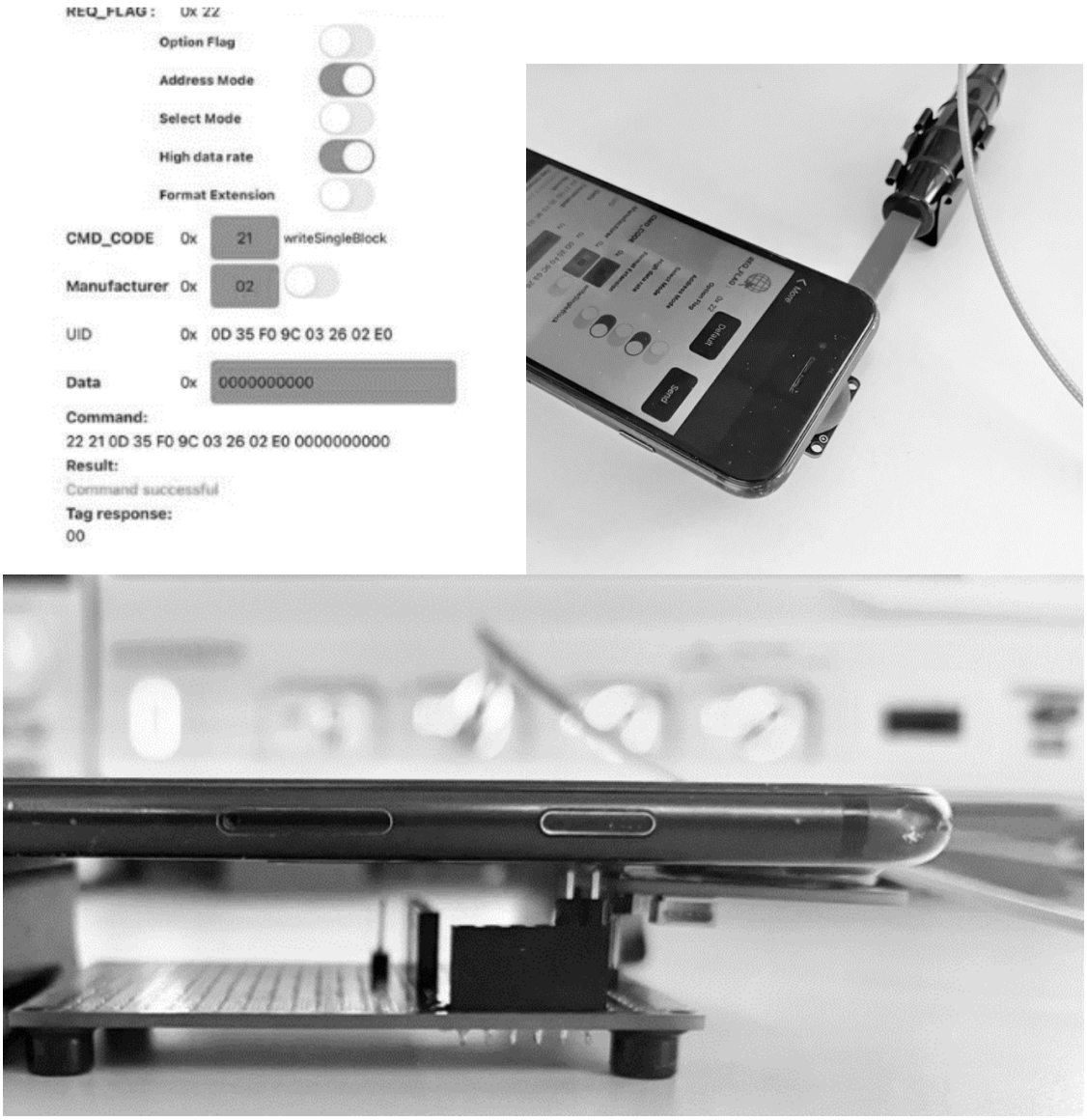

Fig. 7. "Write single block" command waveform capture setup

A smartphone acts as the Vicinity Coupling Device (VCD) [7], generating an NFC request frame using ISO 15693 protocol. Rather than placing the phone over a physical tag, an electromagnetic interference (EMI) probe is positioned near the phone's NFC antenna. The EMI probe is designed to detect high-frequency magnetic field variations, such as the 13.56 MHz carrier used in NFC systems.

The probe is connected via coaxial cable to a high-bandwidth oscilloscope. This allows real-time monitoring of the NFC field, capturing both the modulated downlink (reader-to-tag) request and the load-modulated uplink (tag-to-reader) response. The oscilloscope provides detailed visualization of signal structure, timing, and modulation integrity (Fig. 8).

This oscilloscope capture, taken using a Siglent SDS6204A, shows a full RF communication cycle between an ISO/IEC 15693 host and a passive RFID tag. The waveform clearly illustrates both the downlink (request) and uplink (response) phases of the standard reader-tag interaction at 13.56 MHz, the operating frequency defined by ISO 15693. By zooming in a request operation waveform, can see a typical data structure that corresponds to a first three bytes of VCD “Write single block” command (Fig. 9).

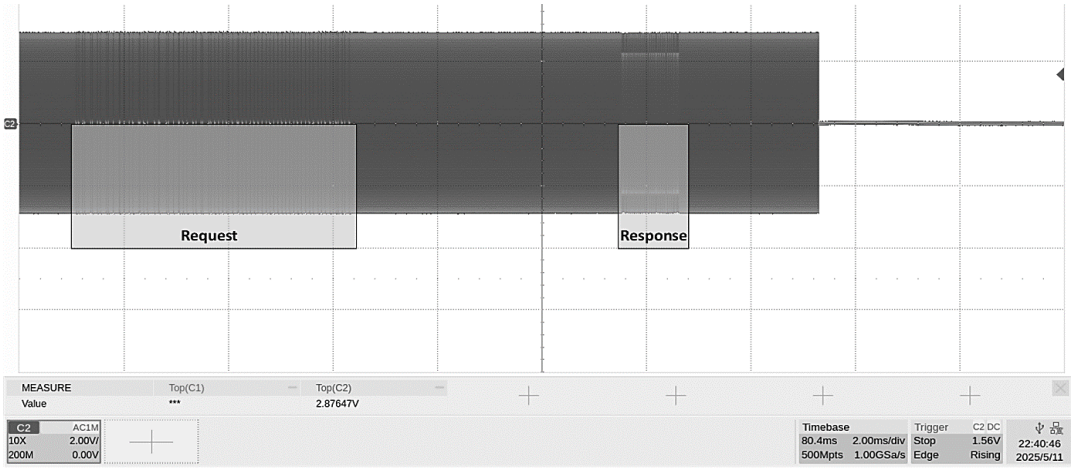

Fig. 8. “Write single block” command waveform

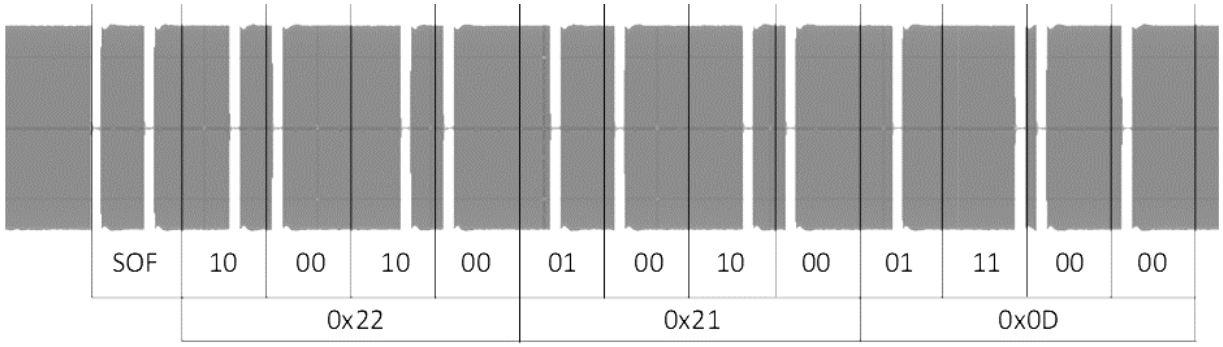

Fig. 9. “Write single block” request part waveform

By zooming in a response operation waveform, in Fig. 10 can see a typical data structure that corresponds to the NFC tag “Write single block” command successful response.

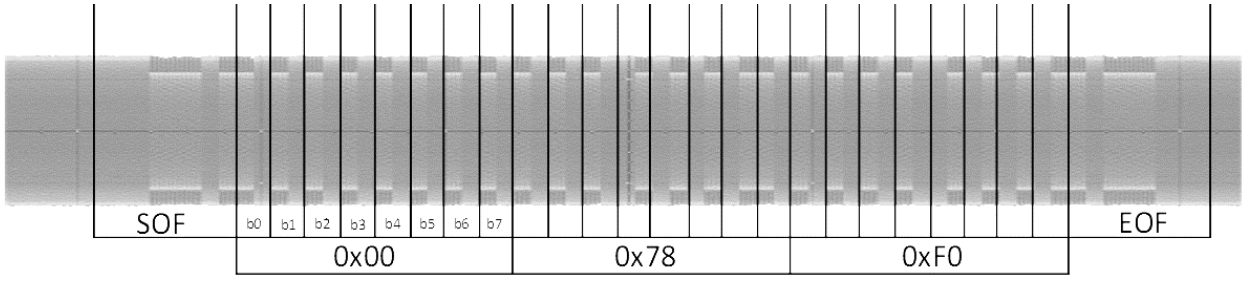

Fig. 10. “Write single block” response part waveform

This demonstration successfully validates the use of ISO/IEC 15693 NFC communication for EEPROM memory operations using the “Write Single Block” command. The experimental setup, comprising a smartphone as the Vicinity Coupling Device (VCD) and a high-resolution signal monitoring system built with an EMI probe and Siglent SDS6204A oscilloscope, enabled accurate observation of both the request and response phases at the physical layer. Detailed waveform analysis confirmed correct frame structuring with clearly identifiable Start of Frame (SOF) and End of Frame (EOF) markers, as well as precise pulse position modulation corresponding to the transmitted data. The downlink was successfully decoded to show the expected 0x22, 0x21, and first byte of UID, matching the “Write Single Block” protocol specification. The uplink confirmed a successful response (0x00), indicating that the EEPROM block at address 0x00 was correctly updated. The use of an EMI probe allowed for non-invasive, high-fidelity capture of the 13.56 MHz carrier and its modulation, providing a robust method for analysing RF behaviour in real time. This approach is especially valuable in NFC debugging, protocol validation, and system integration tasks where direct probing of the tag is not possible. Overall, the test demonstrates a fully functional ISO 15693 NFC-V write operation, verifies correct handling of timing constraints such as EOF isolation, and confirms reliable communication between a commercial smartphone and a passive RFID tag under high data rate conditions.

PLC Host is implemented as a compact transmitter system that combines amplitude modulation, power supply, and wireless configurability. Built on a prototyping board, it enables ASK-modulated data transmission over a shared DC power line to downstream nodes.

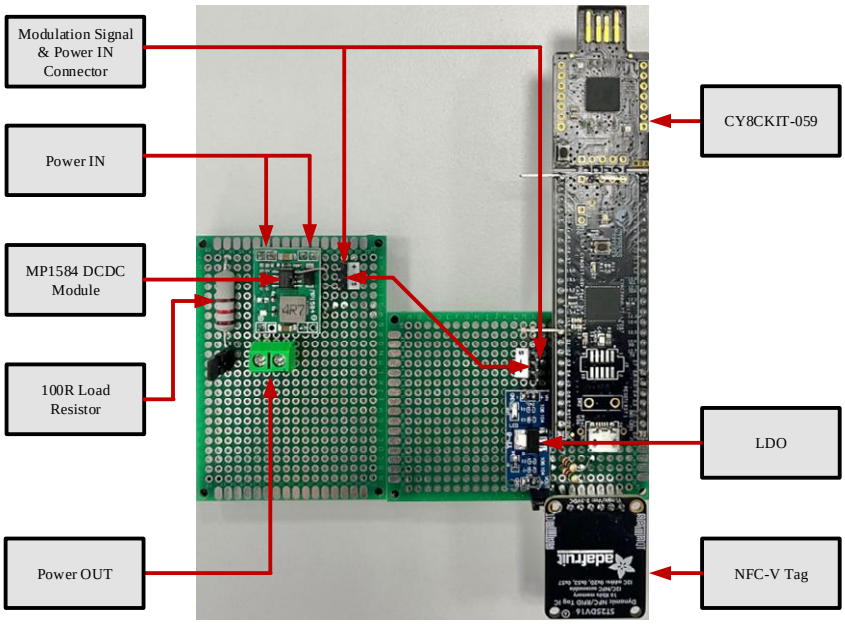

Fig. 11. PLC host prototype

Power and modulation are fed into the system through a common input connector. The incoming signal is routed to an MP1584 step down converter feedback, which regulates the voltage and provides a stable modulated output through the “Power OUT” terminal. A 100Ω resistor serves as a load to stabilize and simulate typical system operation.

The modulation function is handled by a PSoC 5 microcontroller, deployed using the CY8CKIT-059 development board. This microcontroller reads data from EEPROM memory and generates an Amplitude Shift Keying (ASK) signal that is superimposed on the DC power line. The data used for modulation is stored in the NFC-V Tag’s EEPROM and can be updated dynamically with the help of VCD device.

In this system, a PSoC 5LP microcontroller CY8C5888LTI-LP097 is configured to generate an analog output voltage through its internal 8-bit Voltage Digital-to-Analog Converter. The analog voltage

level is controlled via I2C communication initiated by an external master device. Within the firmware design, the microcontroller sends digital commands over the I2C interface, where the data (SDA) and clock (SCL) lines are connected to pins P2 [6] and P2 [7], respectively. These pins are configured to operate in I2C master mode, allowing the device to receive data values from the host controller. Once a digital value is received via the I2C interface, it is forwarded to the VDAC8 peripheral, which converts the 8-bit digital input into a corresponding analog voltage. The system's architecture allows seamless digital-to-analog conversion, enabling the host to dynamically control analog parameters without physical interaction.

The microcontroller is powered using separate analog and digital supply domains to maintain proper operation and noise isolation between functional blocks. This type of configuration is useful in applications requiring programmable analog output, such as sensor simulation, voltage reference generation, or analog modulation, all controlled through a simple two-wire digital interface.

The Embedded firmware routine used in a PSoC 5LP-based system generates an ASK (Amplitude Shift Keying) modulated signal. The design combines analog waveform generation using a DAC with digital control provided via an I2C interface and EEPROM-based configuration. The microcontroller used is the CY8C5888LTI-LP097, which includes integrated I2C communication and an 8-bit VDAC module capable of producing analog voltage levels from a digital lookup table.

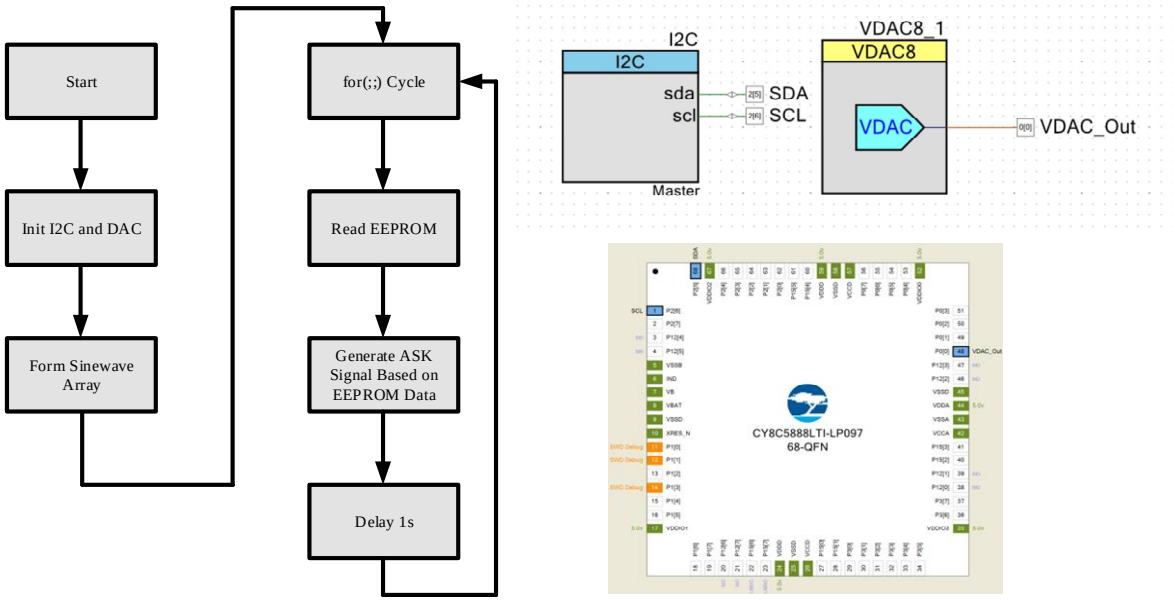

Fig. 12. PLC host embedded workflow

The program execution begins with an initialization phase where both the I2C interface and the DAC peripheral are set up. The I2C bus, connected through pins P2 [6] and P2 [7], enables external access to the EEPROM. This non-volatile memory holds the modulation data that defines the ASK signal characteristics. Once the hardware interfaces are initialized, the firmware constructs a digital sine wave array. This array, stored in memory, contains discrete amplitude values that represent one full cycle of a sine wave. These values will later be streamed to the DAC to synthesize a continuous analog waveform. After this setup, the program enters an infinite loop, ensuring continuous operation. In each cycle, the microcontroller reads the current modulation data from the EEPROM using the I2C interface. This data may encode the on/off keying pattern or amplitude control logic that determines which portions of the sine wave are transmitted and which are suppressed, thus forming an ASK-modulated output. The VDAC8 block receives the appropriate values from the sine wave array based on this logic, converting them into corresponding analog voltages. The analog signal is then output through pin P0 [0], which has been configured as the DAC output.

To manage timing and ensure repeatable output intervals, the system incorporates a 1-second delay after each modulation cycle. This delay acts as a transmission pacing mechanism, allowing the system to periodically refresh the ASK signal based on updated EEPROM content.

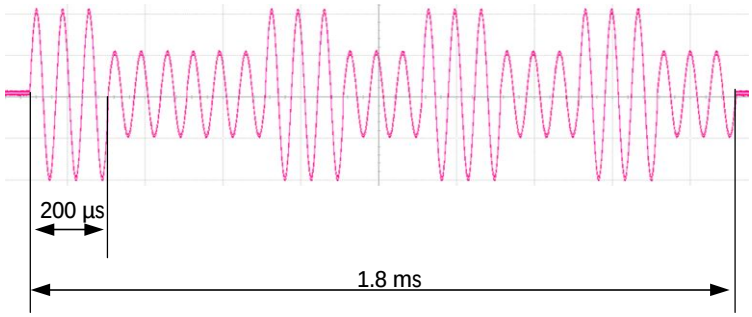

Fig. 13. PLC host analog waveform representation

The waveform shown is a time-domain representation of an Amplitude Shift Keying (ASK) modulated signal generated by the PSoC 5LP system described earlier. The signal consists of a sinusoidal carrier whose amplitude is modulated according to digital data retrieved from EEPROM memory.

The horizontal axis represents time, with the total waveform duration extending over 1.8 milliseconds. The first 200 microseconds and the final part of the waveform exhibit a flat baseline, indicating the absence of a carrier signal, which corresponds to a logical “0” in ASK modulation. Between these zero-amplitude sections lies the modulated portion of the signal, where a continuous sine wave is present. This region spans approximately 1.6 milliseconds and demonstrates multiple cycles of a high-frequency carrier whose amplitude likely varies based on the corresponding EEPROM content.

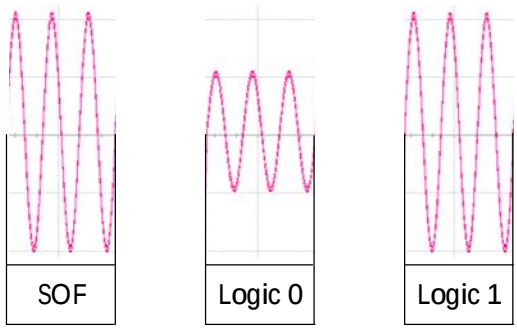

Fig. 14. PLC host analog waveform coding diagram

The image presents three segments of an ASK (Amplitude Shift Keying) modulated waveform, each representing a distinct symbol used in the encoding scheme implemented by the PSoC 5LP system. This waveform is generated using a precomputed sine wave array and selectively output through the internal DAC based on EEPROM data, forming the structure of the transmitted message. The first segment is labelled SOF, which stands for *Start of Frame*. This burst of sine wave cycles serves as a synchronization pattern, alerting the receiving system to the beginning of a new data frame. The amplitude and duration of the SOF pattern are consistent and distinct, allowing it to be easily detected by a demodulation routine. The second segment, labelled Logic 0, shows a group of sine wave cycles with noticeably lower amplitude. This reduction in amplitude is deliberate and encodes a logical zero according to the ASK modulation scheme. By gating the output waveform or scaling the DAC values for this portion, the transmitter differentiates it from other symbols. The third segment, labelled as Logic 1, displays a burst of sine waves at full amplitude, corresponding to a logical one. The higher amplitude makes this symbol distinguishable from Logic 0 and maintains symmetry with the Start of Frame signal, which may share a similar amplitude envelope.

Together, these three waveform segments demonstrate how digital bits and framing information are encoded into an analog waveform through amplitude variations of a carrier signal. This encoding technique enables digital communication over analog channels, such as a DC power line or capacitive coupling path, using only a DAC output and timing control implemented in firmware.

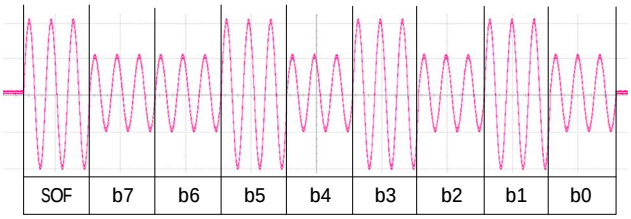

Fig. 15. Transmission word example, value in hex-2A

The Waveform in Fig. 15 illustrates the transmission of an 8-bit data frame using ASK (Amplitude Shift Keying) modulation as implemented in the described PSoC 5LP-based communication system. The waveform is divided into distinct segments, each corresponding to a specific part of the transmission protocol. The process begins with a Start of Frame (SOF) segment, which is represented by a high-amplitude sine wave burst. The SOF acts as a synchronization header, informing the receiver that valid data transmission is about to follow. Following the SOF, the transmission proceeds with the data byte, which is transmitted bit by bit from the most significant bit (b7) to the least significant bit (b0). Each bit is encoded using ASK, where a full-amplitude sine wave represents a logic “1” and a reduced-amplitude sine wave represents a logic “0”’. This modulation scheme allows the receiver to distinguish between binary values by simply comparing the amplitude of each carrier burst within its respective time slot. The precise timing and shaping of each burst are managed by the DAC in the PSoC device, which outputs values from a preloaded sine wave array in synchronization with the EEPROM-defined data. The entire process demonstrates a compact, self-sufficient digital-to-analog transmission system capable of low-speed data signalling over analog channels.

The PLC host system functions as a standard buck converter during power-up, converting a higher DC input voltage to a regulated lower output.

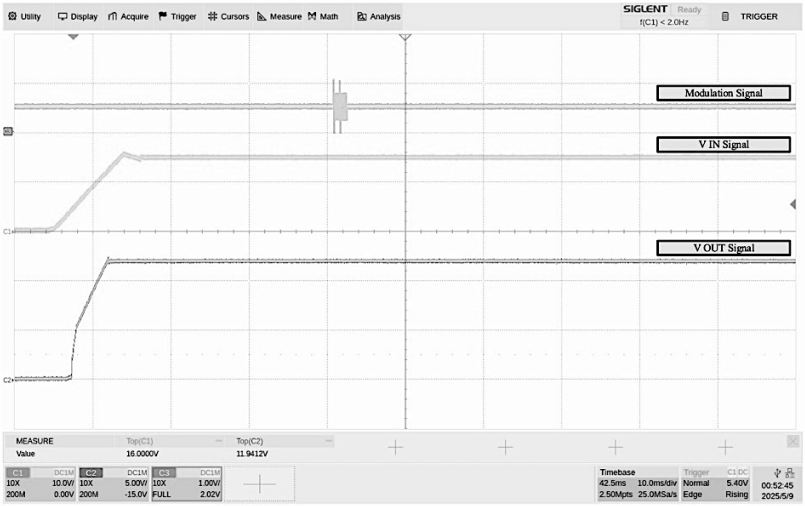

Fig. 16. PLC host operating waveform

Once the converter reaches steady state, the PLC communication is initiated by injecting a high-frequency ASK-modulated signal onto the output line. This modulated signal appears as a brief burst of high-frequency ripple superimposed on the otherwise stable DC voltage. In the waveform, it is visible as a

cluster of rapid oscillations that briefly disturb the flat DC level, corresponding to digital data encoded by turning the carrier on and off (amplitude modulation). The rest of the output remains clean, indicating that communication occurs only during defined intervals, without affecting the power delivery function.

Modulation Signal trace shows a short burst of high frequency ASK modulation superimposed on the steady DC level of the output rail. This modulated waveform represents digital data being transmitted over the power line using the output ripple as a carrier. The input voltage ramps from 0 V to a final level of 16.0 V. The controlled and gradual nature of the ramp suggests soft-start behaviour, typical of a buck converter designed to limit inrush current and ensure smooth start-up. The output voltage of the converter rises to and stabilizes at approximately 11.94 V. This output corresponds to a typical step-down conversion from the 16 V input and exhibits excellent regulation. The waveform is clean and shows no significant oscillations or overshoot, apart from a brief segment where the ASK modulation is visible.

Performing a Fast Fourier Transform (FFT) on a signal is essential when need to analyse frequency content. In the context of a DC-DC converter with superimposed communication – like a power line communication system – FFT is especially valuable for several reasons: identify modulation components, distinguish power and communication spectrum, noise and harmonic analysis, demodulation and decoding aid, debugging and compliance. FFT helps detect the frequency and amplitude of the ASK-modulated carrier signal. Since ASK involves toggling a carrier frequency on and off, FFT can reveal this carrier as a distinct spectral peak, confirming the presence and integrity of the modulation. The DC-DC converter's switching frequency typically dominates the lower part of the spectrum. FFT analysis allows engineers to verify that the communication signal (often in a higher frequency band) does not interfere with the converter's normal operation and vice versa.

If the receiver uses frequency-domain filtering or detection, the FFT provides a practical view of how well the signal stands out from the noise floor. It helps design band-pass filters and detect symbol transitions more robustly. FFT makes it possible to identify and quantify noise components, harmonic distortion, and unwanted spurious signals. This is crucial for optimizing signal-to-noise ratio (SNR) and minimizing total harmonic distortion (THD), which affect both power quality and communication reliability.

$$THD + N = 100\% * \frac{\sqrt{V_{sig\_2}^2 + V_{sig\_3}^2 + ... + V_{sig\_n}^2 + V_{noise\_1}^2 + V_{noise\_2}^2 + ... + V_{noise\_n}^2}}{V_{sig\_1}}, \quad (1)$$

where V_{sig_1} – fundamental harmonic amplitude in V_{RMS}; V_{sig_2} – second harmonic of fundamental signal amplitude in V_{RMS}; V_{noice_n} – amplitude of each noise harmonics in $V_{RMS.}$

$$V_{RMD} = 10^{\frac{dBV}{20}},$$

$$SNR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right), \quad (2)$$

$$\frac{P_{signal}}{P_{noise}} = \frac{V_{RMS\_signal}^2}{V_{RMS\_noise}^2} = \frac{V_{sig\_2}^2 + V_{sig\_3}^2 + ... + V_{sig\_n}^2}{V_{noise\_1}^2 + V_{noise\_2}^2 + ... + V_{noise\_n}^2},$$

where P_{signal} – carrier signal power in *W*; P_{niose} – noise power in carrier signal spectrum in *W*.

The Power Line Communication modulator setup represents the first signal pass stage of the undergoing validation on a laboratory test bench. At this stage, the primary objective is to verify the generation and integrity of the modulated signal prior before it injects into the power line.

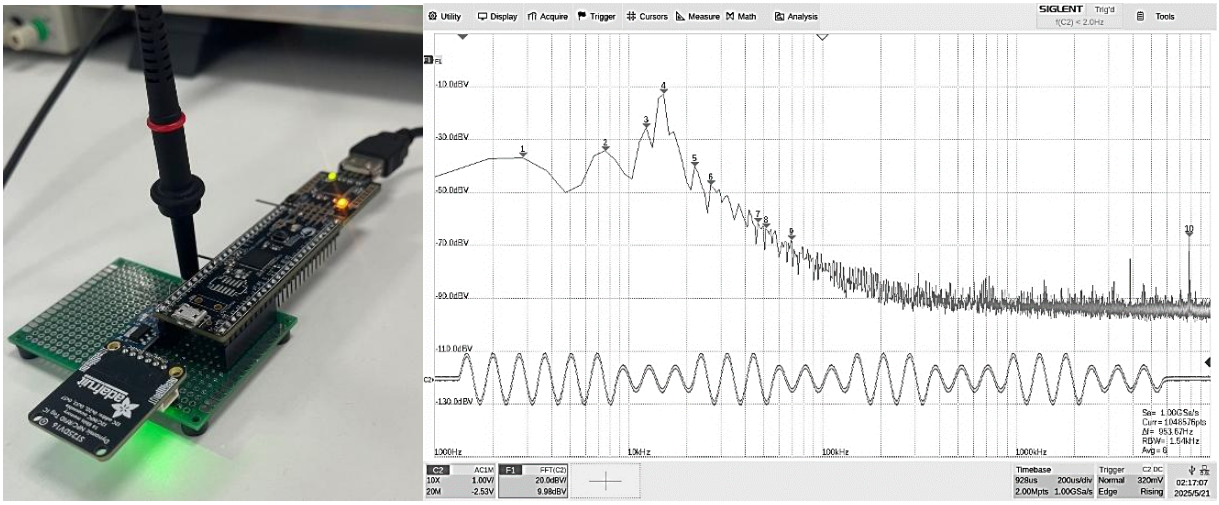

Fig. 17. PLC injection signal waveform and FFT, THD+N =4.8

The modulator hardware is implemented using a microcontroller development board capable of generating a carrier waveform and applying amplitude shift keying (ASK) modulation. This is the initial analog output produced directly by the modulator's digital or mixed-signal block. A probe connected to the oscilloscope captures this signal for both time-domain and spectral analysis. The oscilloscope displays waveform corresponding to the time-domain view of the ASK-modulated signal. The clear periodic structure with amplitude variations confirms successful carrier generation and baseband modulation. The amplitude of Logic 1 is 1.024 $V_{p\text{-}p}$, Logic 0 is represented as 0.512 $V_{p\text{-}p}$ sinewave. This waveform reflects the raw output of the modulator before any signal conditioning. The upper FFT trace reveals the signal's spectral composition. The sinewave is still digitalized, as it is generated by VDAC block. The spectrum looks quiet flat. The harmonics "10" shows a discretization frequency, that corresponds to DAC output value update. The amplitude distribution across frequencies allows the evaluation of spectral purity, harmonic distortion, and signal-to-noise characteristics.

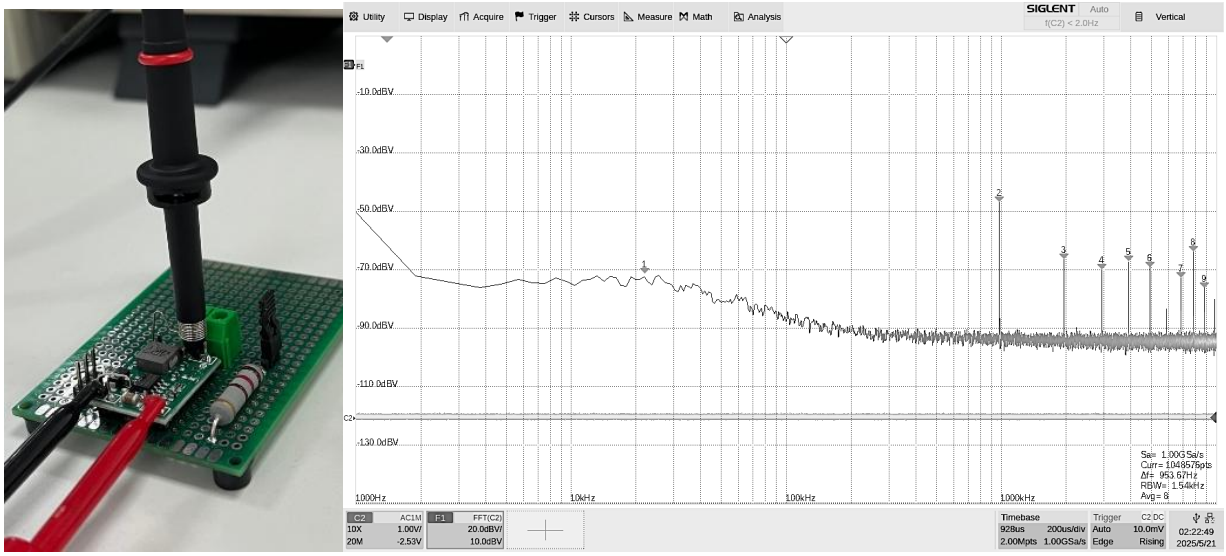

Fig. 18. Unmodulated DC-DC signal waveform and FFT

The second stage of the Power Line Communication is evaluated as a DC-DC converter system, focusing on output spectral integrity and noise behaviour. The setup shows an unmodulated DCDC output spectrum. The hardware under test is a buck converter operating under typical load conditions, assembled on a prototyping platform.

The oscilloscope probe is used to measure the converter's output directly, capturing the resulting voltage waveform for frequency-domain analysis. In frequency range from 10 kHz to 900 kHz spectrum looks mostly flat. The noise harmonics starting from 990 kHz, frequency range domain. Fundamentally, the selected DCDC converter MP1584 operates within a switching frequency range of 100 kHz to 1.5 MHz This flexibility is achieved by configuring an external resistor. The PLC system works on 990 kHz switching frequency.

After the ASK signal injection, the SNR ratio significantly increase. The measurement represents the raw signal acquired from a Power Line Communication (PLC) system during its early transmission stage. In this process, a modulated signal is actively injected onto a DC power line using a microcontroller-based modulator circuit. The transmission occurs by superimposing an ASK-modulated carrier onto the power rail, typically within the tens of kilohertz range, to enable data communication without disrupting the primary power delivery.

During signal acquisition, an oscilloscope is used to capture both the time-domain waveform and its corresponding frequency-domain representation using a Fast Fourier Transform (FFT). The time-domain view reveals periodic oscillations resulting from the ASK modulation, which are embedded within the DC bias. The FFT analysis highlights a dominant spectral component cantered around 14.8 kHz, corresponding to the carrier frequency. Additional harmonic components are observed at integer multiples of the carrier, indicating nonlinearities and possible spectral distortion.

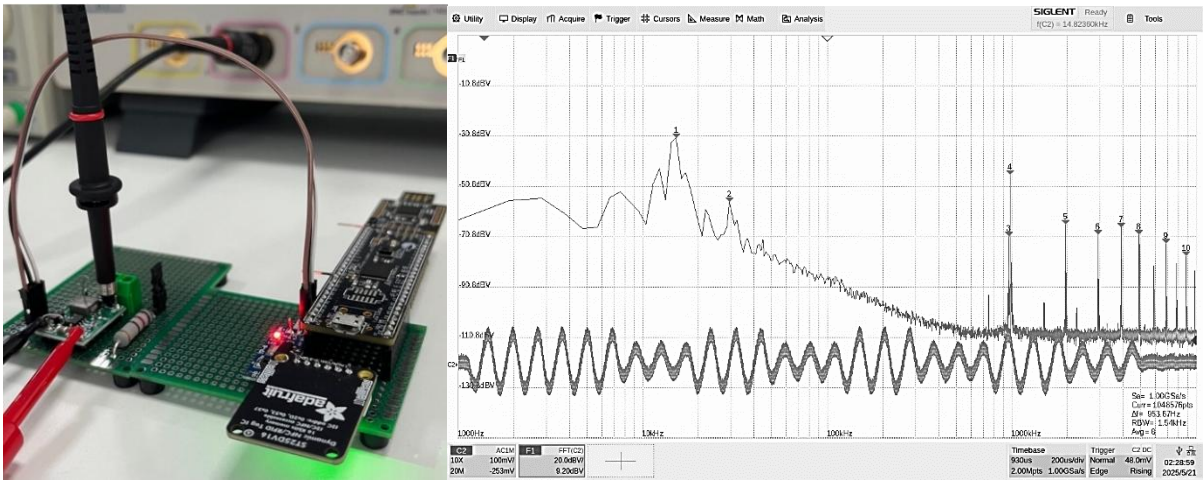

Fig. 19. Modulated DC-DC signal waveform and FFT. THD+N =19.6 %, SNR = 14.5 dB

From a signal integrity perspective, the Signal-to-Noise Ratio (SNR) is a critical performance metric. It is evaluated by comparing the power of the fundamental signal component to the surrounding noise floor. In this case, the noise level remains significantly lower than the main peak, yielding a high SNR indicative of a strong and detectable signal. However, the presence of elevated harmonics suggests some degree of distortion, likely introduced by switching noise or parasitic impedance in the modulation circuit. These distortions may impair the reliability of symbol detection, particularly under varying load or line conditions. This measurement phase serves to validate the strength, purity, and spectral composition of the transmitted signal before downstream processing or demodulation. It is a foundational step in characterizing PLC system behaviour and guiding further refinement of the modulation hardware and filtering strategy.

3. The PLC node overview

On the other side of PLC communication system stays a PLC node. It operates by extracting both power and data from a single two-wire line carrying a +12 V DC supply with superimposed ASK-modulated communication signals. Upon entry, the +12 V line is directed into two parallel processing paths. The first path supplies energy to a step-down DC-DC converter, which generates a regulated +5 V output.

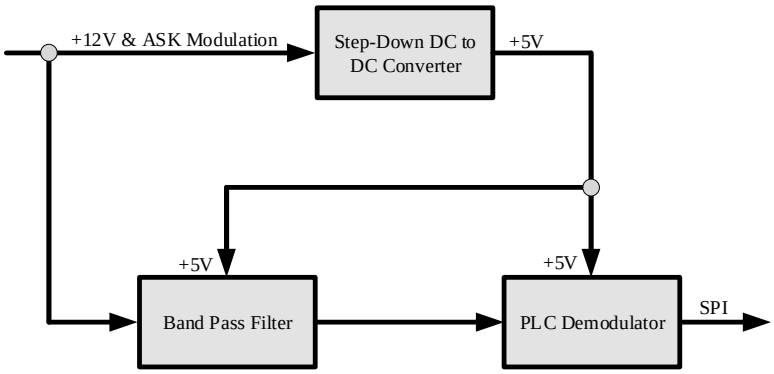

Fig. 20. PLC node block diagram

This regulated voltage is used to power the subsequent functional blocks within the node, ensuring stable operation regardless of minor fluctuations in the input voltage. The second path handles the communication aspect. The combined power and modulation signal is routed to a band-pass filter that is designed to isolate the frequency band used for ASK modulation. This filtering stage suppresses the low-frequency DC component and broadband noise, allowing only the desired carrier frequency and its modulated envelope to pass through. This stage is critical for preserving signal integrity and reducing distortion prior to demodulation. The filtered signal is then processed by the PLC demodulator, which recovers the original digital data encoded in the amplitude variations of the carrier. The demodulated data is output via an SPI interface for integration into higher-level control or monitoring systems.

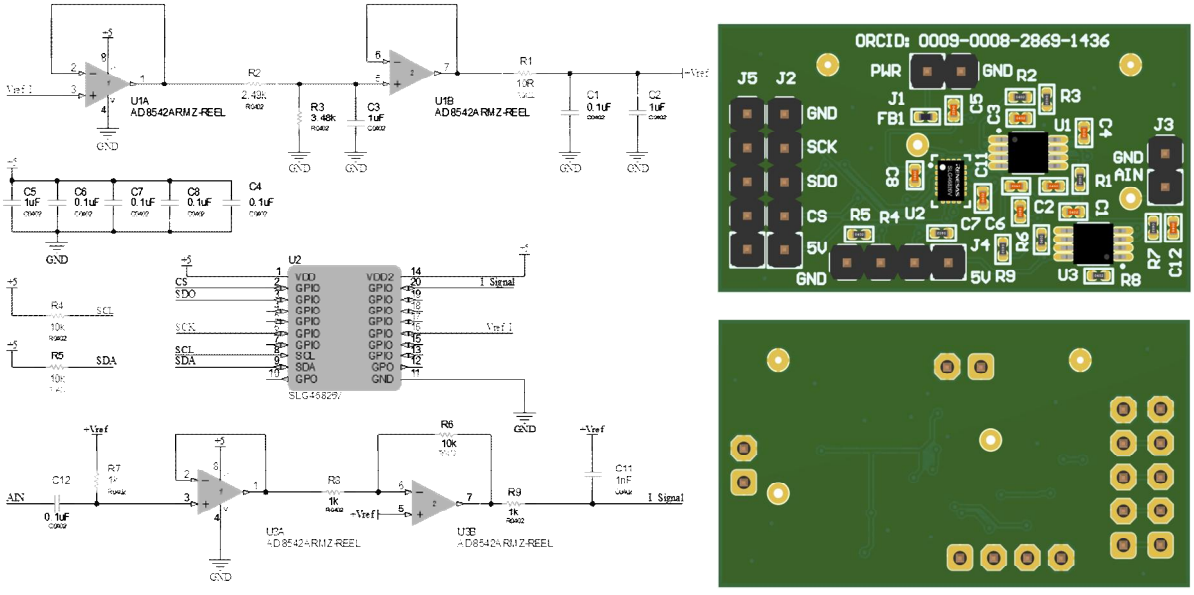

Fig. 21. BPF board with schematic diagram

The Filter stage of the PLC system is responsible for filtering and signal decoding. It performs two essential functions: suppression of high-frequency switching noise originating from the DC-DC power converter, and AC coupling to block the DC component of the power line while preserving the modulated communication signal. The analog front-end includes a carefully designed active band-pass filter implemented with precision operational amplifiers. This filter attenuates low-frequency and high-frequency components, allowing only the frequency band containing the ASK-modulated carrier to pass through. Additionally, the AC coupling capacitors remove the DC offset, ensuring that only the communication signal is presented to the decoding logic.

The filtered signal is then processed by a configurable GreenPAK IC, which utilizes internal comparators to detect amplitude transitions and reconstruct the original digital data. These comparators convert the analog ASK envelope into a digital stream suitable for further communication, typically interfaced via SPI or similar protocol. The GreenPAK device offers a programmable logic environment, enabling the integration of comparator thresholds, logic gating, and basic timing without the need for external digital ICs.

This block is crucial for reliable PLC reception, as it isolates the signal from power delivery noise and translates the analog modulation into a clean, logic-level representation for system-level data handling.

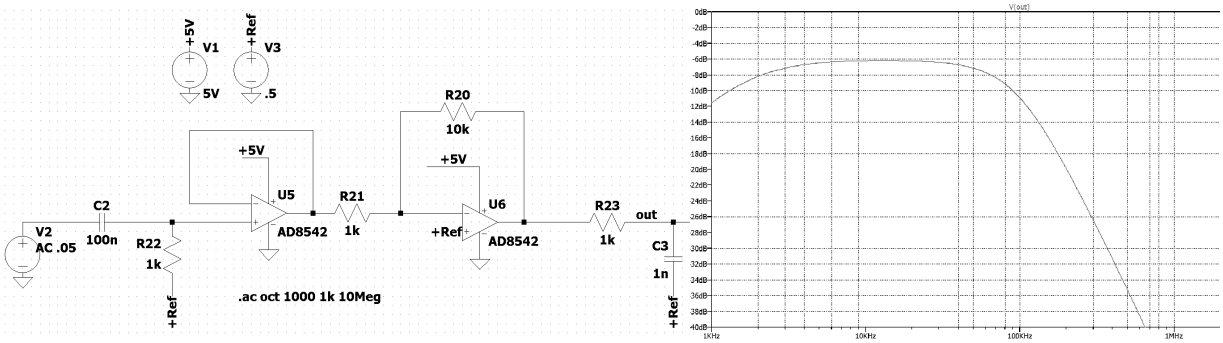

Fig. 22. BPF simulation setup

To design and characterize this filter, an initial simulation was carried out as the first step in the development process. The simulation setup demonstrates the behaviour of a first-order active band-pass filter designed specifically for a PLC receiver front end. The filter's centre frequency is set at 15 kHz, corresponding to the carrier frequency used in the ASK-modulated communication signal.

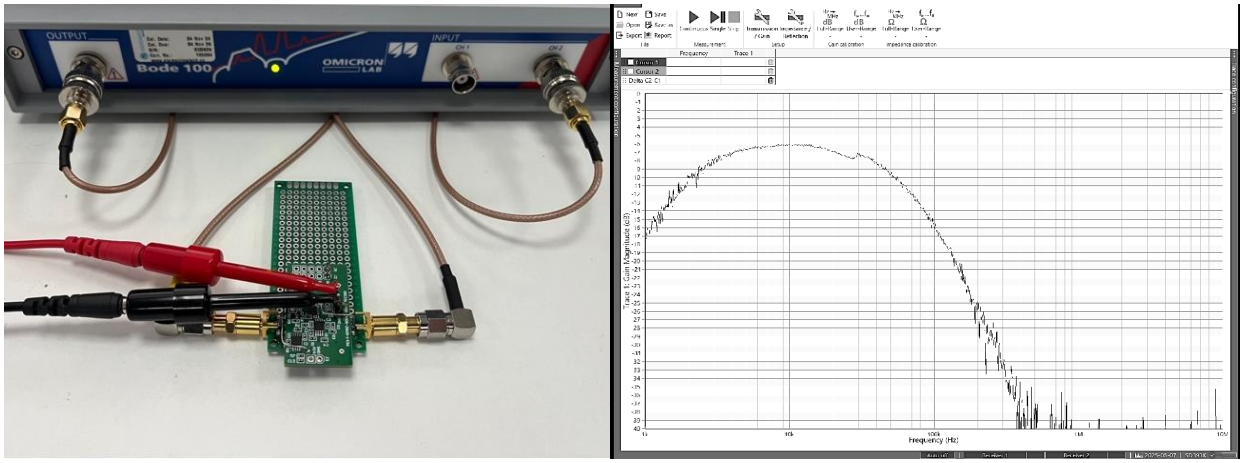

Fig. 23. BPF block measurement setup

The circuit employs two cascaded operational amplifiers configured to perform both high-pass and low-pass filtering actions. The first stage provides AC coupling and high-pass filtering to remove the DC offset and suppress low-frequency noise, while the second stage implements a low-pass function to attenuate higher-

frequency components such as switching transients from the DC-DC converter or electromagnetic interference. This type of first-order analog filtering stage is particularly important in power line communication systems where signal integrity must be maintained in the presence of noise and varying power conditions, ensuring reliable demodulation in downstream processing stages.This setup represents the bench evaluation process of a first-order analog band-pass filter developed for a PLC receiver. The goal of this procedure is to experimentally validate the frequency response characteristics that were previously verified through simulation.

The filter under test was initially designed with a centre frequency of 15 kHz, targeting selective amplification of ASK-modulated signals typical in PLC applications. In simulation, the circuit demonstrated a band-pass response with flat gain near 15 kHz and attenuation at both lower and higher frequencies. The design incorporated AC coupling and active filtering stages to suppress the DC offset and reject unwanted spectral content originating from sources such as DC-DC converter noise. For physical characterization, a vector network analyser (VNA) is used to measure the gain across a broad frequency range. The filter is powered and connected via SMA interfaces, and the VNA applies a swept-frequency test signal while measuring the corresponding output amplitude. The plot displayed on the right confirms the expected band-pass behaviour, with a gain peak cantered near the target frequency and a consistent roll-off beyond the passband.

This empirical result closely aligns with the simulation output, validating the design's effectiveness and confirming that the filter reliably passes the desired PLC communication band while attenuating out-of-band disturbances. This step is critical in transitioning from theoretical design to practical deployment, ensuring predictable signal integrity in real-world operating environments.

In comparison to the simulation, the measured frequency response on the bench exhibits a similar overall shape and confirms the expected band-pass behaviour cantered around 15 kHz. The peak gain, roll-off slopes, and bandwidth closely match the simulated results, demonstrating that the filter operates as designed under real conditions.

Minor discrepancies between the simulated and measured plots are attributed to tolerances in the passive component values used in the physical circuit. Specifically, the capacitors in the filter network have a tolerance of ±20 %, while the resistors have a tighter deviation of ±1 %. These variations slightly shift the filter's corner frequencies and may also affect the peak gain and symmetry of the response. Despite these inherent tolerances, the experimental result remains within acceptable margins and validates the robustness of the design for its intended PLC application.

The last step of the bench evaluation process for the PLC receiver subsystem is shown in Fig. 24. At this point, the system is fully assembled and operational, and the focus is on verifying the integrity of the filtered signal that has traversed the analog front end.

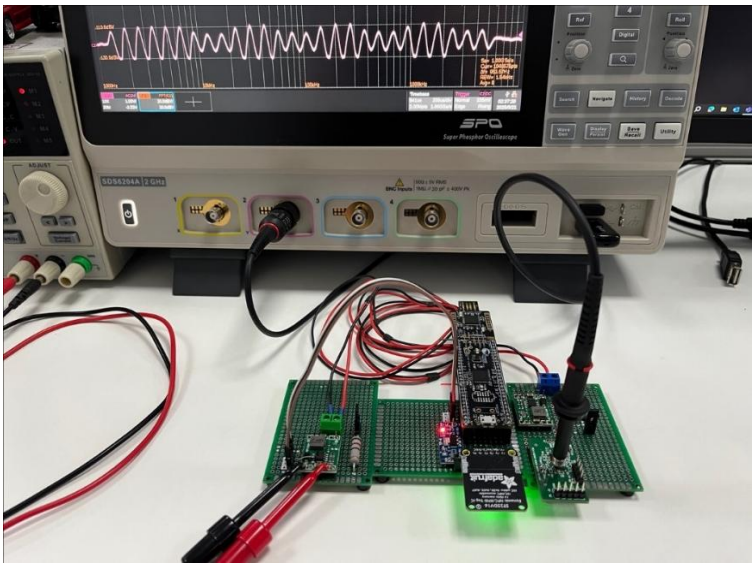

Fig. 24. PLC host to PLC node signal quality measurement setup

A modulated signal containing an ASK carrier is injected onto the power line, passing through the designed band-pass filter. The output of the filter is then probed and observed using a high-bandwidth oscilloscope. The waveform displayed confirms the successful recovery of the carrier envelope, demonstrating clear amplitude modulation characteristics. The captured signal represents the return path after filtering, where low-frequency power rail fluctuations and high-frequency switching noise have been effectively attenuated. Only the desired communication band – cantered around 15 kHz – is preserved. This clean, demodulation-ready waveform is essential for ensuring reliable symbol decoding in the subsequent digital stage. This measurement validates that the analog front end performs as expected under real operating conditions, including actual power supply interference and component tolerances. It confirms the combined effect of AC coupling, band-limiting, and amplifier stages in preparing the signal for digital interpretation by the comparator-based decoding circuit. The result ensures that the system is ready for deployment in power line communication applications where robustness and signal fidelity are critical.

The bench measurement setup was conducted to obtain the spectrum of the return signal after it passed through the analog front end. This evaluation aimed to verify the effectiveness of the filtering stage in isolating the modulated carrier from noise sources, particularly those introduced by the DC-DC converter. By capturing the frequency-domain representation of the processed signal, it was possible to confirm the suppression of unwanted components and assess the impact of the filter on signal quality, including any distortion or harmonic content introduced during filtering. this spectrum represents the final filtered signal observed at the output of the PLC analog front end. It shows the frequency-domain and time-domain characteristics of the ASK-modulated carrier after passing through the custom-designed band-pass filter. The primary spectral peak is located at approximately 14.1 kHz, corresponding to the target modulation frequency. The filtering stage effectively suppresses broadband switching noise originating from the DC-DC converter, which was previously present in earlier measurement stages. As a result, the noise floor is significantly reduced, falling below –110 dBV across much of the spectrum, indicating successful removal of high-frequency interference and low-frequency ripple components.

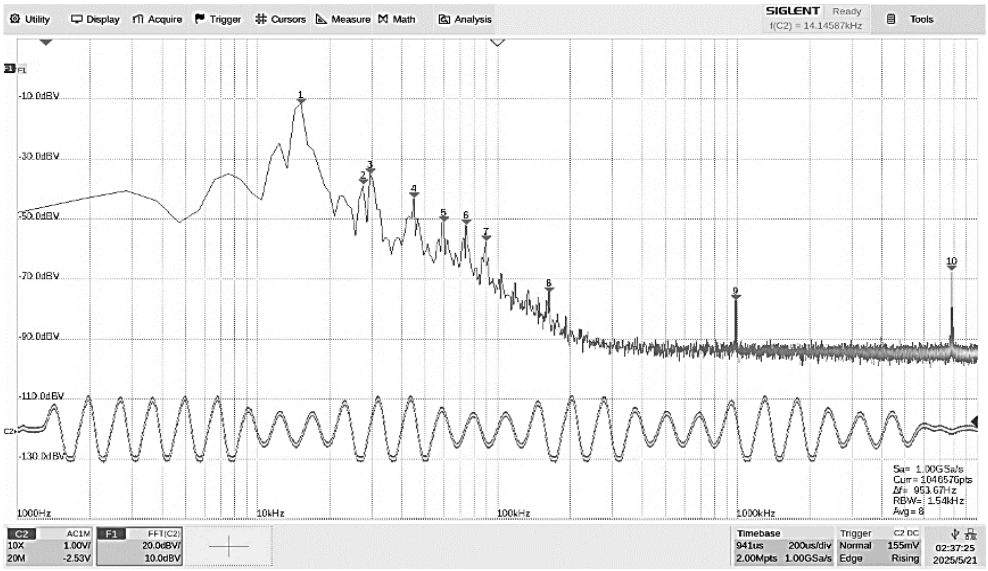

Fig. 25. PLC host to PLC node signal waveform and FFT.
THD+N =8.6 %, SNR = 52.5 dB

A slight increase in total harmonic distortion (THD) is visible, with harmonic components observable at integer multiples of the fundamental frequency. These residual harmonics are likely introduced by the non-linear phase or gain characteristics of the analog filter and active amplifier stages. However, the amplitude of these harmonics remains substantially lower than the fundamental, ensuring

that signal integrity is preserved for reliable digital demodulation. This spectrum validates the performance of the band-pass filter in isolating the desired communication signal while mitigating noise and distortion, thereby confirming the readiness of the analog front end for integration into a complete PLC system.

The GreenPAK IC project implements a custom digital decoding logic that transforms the filtered analog PLC sinewave into a synchronous SPI data stream. The core of this architecture is based on the use of integrated analog comparators, digital counters, delay blocks, and LUT logic to detect and process the modulated signal envelope. The incoming sinewave signal, representing the ASK-modulated PLC data, is fed into two analog comparators. These comparators are referenced to fixed threshold levels – one high (96 mV) and one low (–640 mV) – to capture the zero-crossing and amplitude excursions of the signal. The output of each comparator is then used to clock associated 3-bit counters, which serve to quantify the signal timing and ensure consistent pulse shaping. To mitigate unwanted high-frequency artifacts – specifically a 1 MHz component observed in the frequency domain of the returned PLC signal – each comparator output is passed through a 100 ns digital delay.

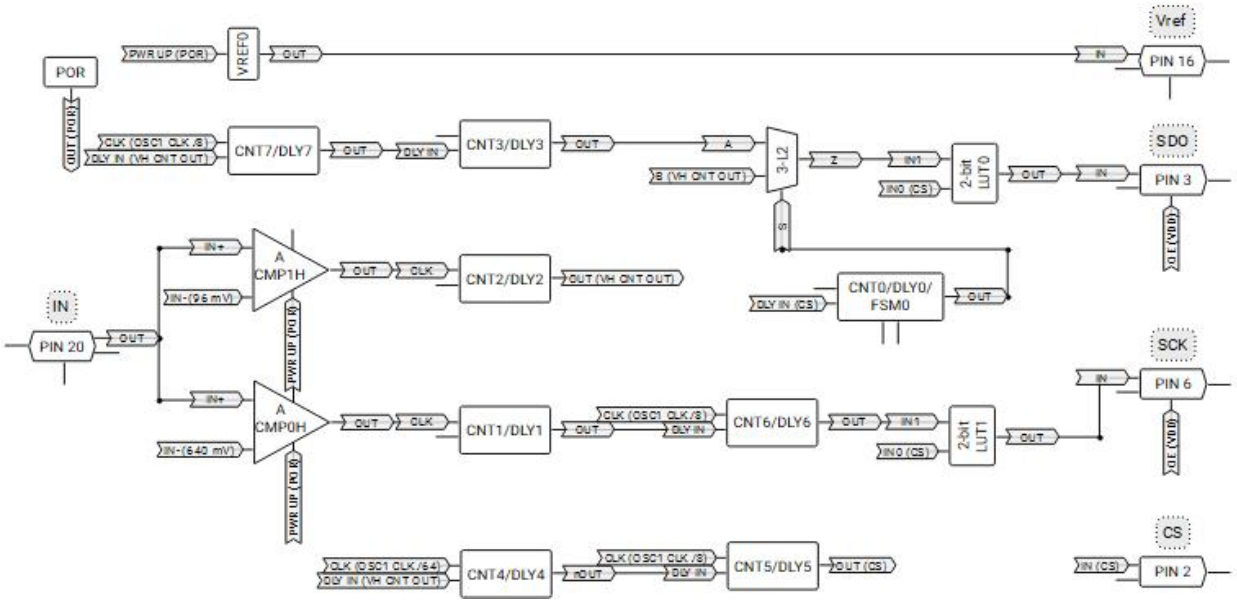

Fig. 26. ASK to SPI decoder design

These delay elements act as temporal filters to suppress fast switching transients that do not carry valid data content. The CS (chip select) signal is derived from a Start-of-Frame (SOF) detection mechanism implemented via a finite state machine (FSM) triggered by specific comparator events. This FSM coordinates the timing for SPI transaction framing. SPI-compatible signals – such as SDO, SCK, and CS – are generated directly by LUTs and output blocks within the GreenPAK configuration. This implementation allows real-time digital decoding of amplitude-modulated PLC waveforms without a traditional microcontroller, enabling efficient signal recovery and serial interfacing in compact, low-power embedded systems.

This setup illustrates the evaluation process of a PLC decoder circuit, which is responsible for converting an amplitude-shift keyed (ASK) signal into a digital data stream. The decoder under test receives a modulated sinewave signal from the power line – previously filtered by the analog front end – and processes it using a combination of comparators, delay blocks, and digital counters.

The oscilloscope captures in the top three quadrants display multiple signal traces that correspond to different stages of the decoding process. The uppermost waveform in each plot shows the modulated ASK signal, which varies in amplitude and duration depending on the encoded data. Beneath it are logic-level signals derived from the decoder's internal timing and logic stages.

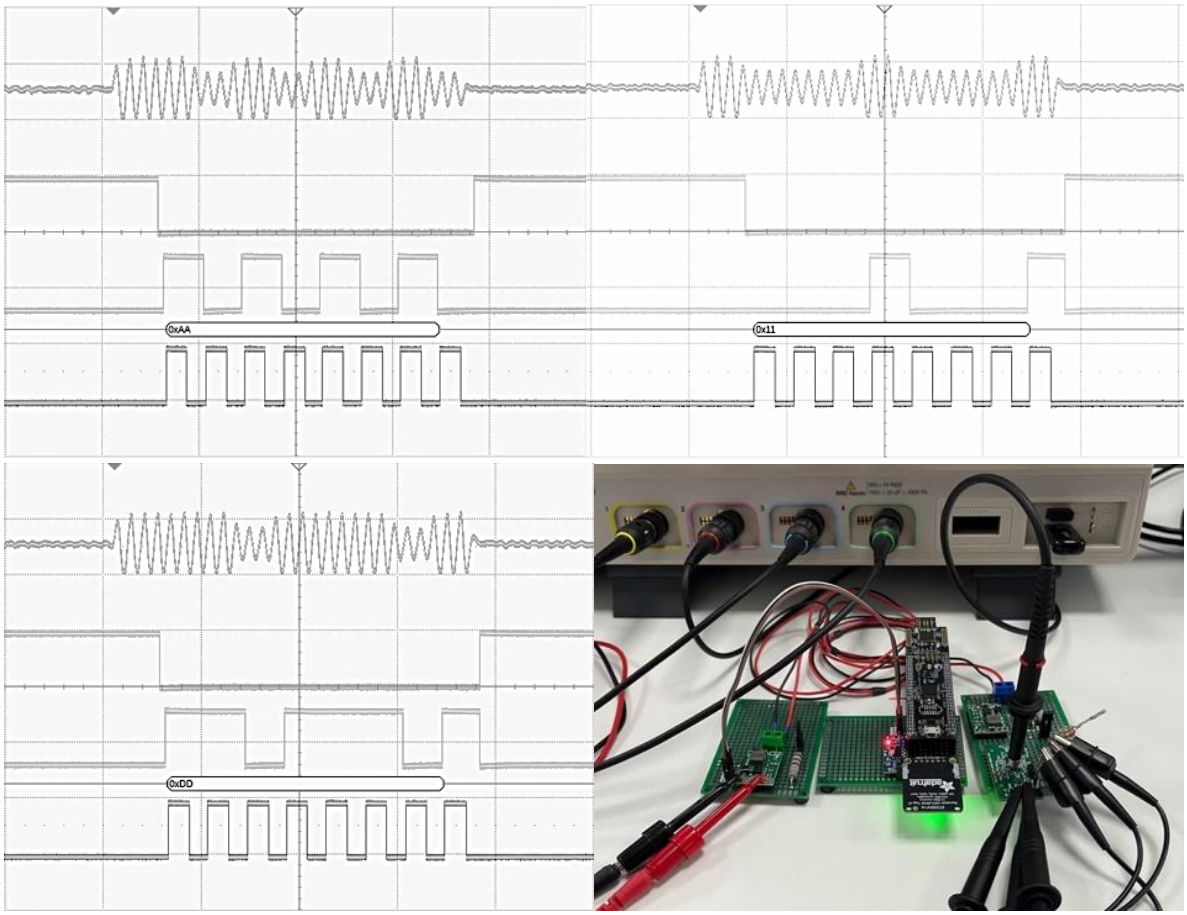

Fig. 27. ASK to SPI decoder bench testing results

The circuit uses analog comparators to detect signal thresholds and mark transitions. These transitions clock digital counters that segment the waveform and extract bit timing. Additional delays and filtering logic are applied to reject unwanted high-frequency artifacts and to enforce temporal coherence. The outputs form a valid digital reconstruction of the original data, presented as SPI-like sequences at the lower part of each capture. Each frame represents a recognized bit pattern, such as 0x1A, 0x11, or 0x4D, indicating successful demodulation of the original message. The bottom-right quadrant of the image shows the bench test environment. The complete PLC receiver chain is assembled and powered, with oscilloscope probes attached at critical signal nodes. The decoder is based on a GreenPAK device, which interprets the incoming analog waveform and generates the synchronized digital output. This evaluation confirms that the decoder is functioning correctly, accurately translating ASK modulated signals into clean digital words. The waveforms demonstrate the decoder's sensitivity to signal timing and amplitude, as well as its robustness against potential noise or distortion from the power line.

Conclusion

The FFT of injected signal in Fig. 28 shows the original ASK-modulated signal prior to any transmission or filtering. The fundamental component is centred at approximately 14.1 kHz, with a clean spectral profile and well-defined harmonic structure. The harmonics visible here, while present, are part of the expected spectral content due to the modulation envelope. The noise floor is relatively low, and the waveform in the time domain exhibits a well-shaped ASK-modulated sinusoid – indicating a high-quality source signal. The FFT of return signal shows the signal after it has propagated through the power line, passed through the analog filter, and been re-acquired for analysis. While the fundamental at 14.1 kHz is preserved and dominant, the harmonic content has been reduced and smoothed.

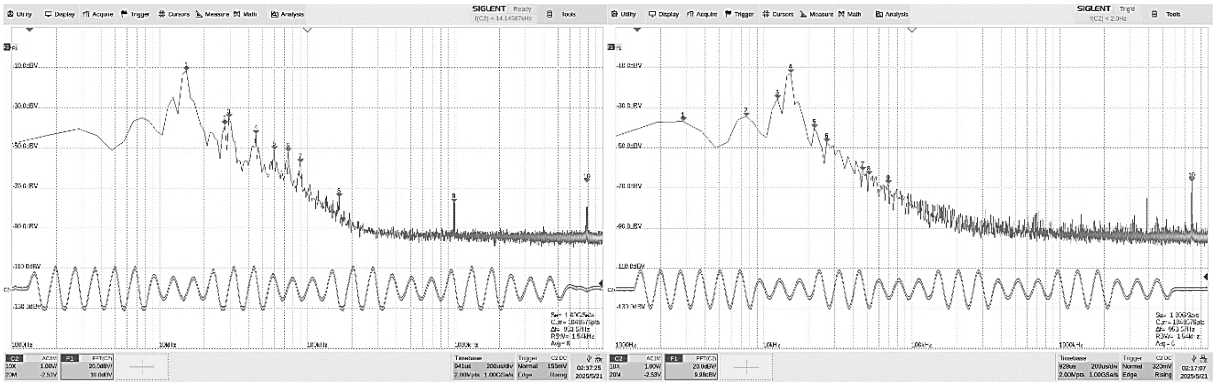

Fig. 28. Comparison between return (on the left) and injected (on the right) signals

The suppression of higher-order harmonics and spurious peaks suggests that the band-pass filter has effectively limited spectral leakage and removed high-frequency noise, particularly from switching sources like the DC-DC converter. However, this filtering introduces a slight total harmonic distortion, observable as a minor loss in harmonic fidelity. The THD increases swing is only 3.8 %. In conclusion, the comparison confirms that the signal remains structurally intact after transmission and filtering. The key modulation frequency is preserved with sufficient amplitude, while noise and high-frequency content have been attenuated. This validates the analog front end's ability to extract and preserve communication content while mitigating interference from the power environment. The return signal spectrum doesn't have any affect in respect to original signal that was injected into the powerline. The signal quality analysis (*THD+N* =8.6 %, *SNR* = 52.5 dB) are demonstrating a high probability of signal capturing even with low quality hardware. Most LDOs have high PSRR parameters in low frequency range, so the power domain of target device on PLC node will not be affected with harmonics, generated by the PLC host.

References

[1] L. Tarasenko and V. Voloskyi, "SWITCHING RIPPLE DATA TRANSFER TECHNIQUE USING STEP-DOWN DC-DC CONVERTER", Information and communication technologies, electronic engineering, Vol. 4, pp. 121–129, 2024. DOI: 10.23939/ictee2024.02.

[2] A. Katsuki, K. Morita, K. Masutomo, and S. Maeyama, "Signal transmission by high-ripple DC-DC converter in a new wire communication system", in 2014 IEEE 36th International Telecommunications Energy Conference (INTELEC), 28 Sept. – 2 Oct. 2014 2014, pp. 1–7. DOI: 10.1109/INTLEC.2014.6972216.

[3] V. Voloskyi, Y. Leshchyshyn, N. Romanyshyn, A. Palamar, and L. Tarasenko, "Method and algorithm for efficient cell balancing in the lithium-ion battery control system", presented at the The 1st International Workshop on Bioinformatics and Applied Information Technologies 2024, Zboriv, Ukraine, 2024 [Online]. Available: https://ceur-ws.org/Vol-3842/.

[4] M. Boada, A. Lazaro, R. Villarino, E. Gil-Dolcet, and D. Girbau, "Battery-Less NFC Bicycle Tire Pressure Sensor Based on a Force-Sensing Resistor", IEEE Access, Vol. 9, pp. 103975–103987, 2021. DOI: 10.1109/ACCESS.2021.3099946.

[5] A. Lazaro, M. Boada, R. Villarino, and D. Girbau, "Study on the Reading of Energy-Harvested Implanted NFC Tags Using Mobile Phones", IEEE Access, Vol. 8, pp. 2200–2221, 2020. DOI: 10.1109/ACCESS.2019.2962570.

[6] J. Kundrata, I. Skeledzija, and A. Baric, "EMI and Voltage Ripple Co-Optimization of a Spread-Spectrum Controller in Buck Converters", IEEE Access, Vol. 10, pp. 131909–131919, 2022. DOI: 10.1109/ACCESS.2022.3229972.

[7] M. S. Chishti, C. T. King, and A. Banerjee, "Exploring Half-Duplex Communication of NFC Read/Write Mode for Secure Multi-Factor Authentication", IEEE Access, Vol. 9, pp. 6344–6357, 2021. DOI: 10.1109/ACCESS.2020.3048711.

PLC СИСТЕМА З NFC КЕРУВАННЯМ ДЛЯ ПРИСТРОЇВ У СФЕРІ ІНТЕРНЕТУ РЕЧЕЙ

Лев Тарасенко

Національний університет "Львівська політехніка", вул. С. Бандери, 12, Львів, 79013, Україна

Технологія передавання даних в мережах постійного струму (PLC) забезпечує передавання інформаційних сигналів через наявні силові лінії, даючи змогу електричним провідникам виконувати подвійну функцію – живлення та передавання даних. Її широко застосовують як у побутових, так і в промислових умовах для створення мереж зв'язку без необхідності в прокладанні додаткових спеціалізованих кабелів. Запропонована технологія може стати ефективною для систем з обмеженим фізичним доступом або для модернізації вже наявних рішень. У цій роботі описано модифікований фізичний рівень комунікацій у мережах PLC. Такий тип обміну данних призначений для роботи із вузлами живлення постійного струму. Передавання даних здійснюється між головним пристроєм PLC і підключеними вузлами. Кожен етап передавання сигналу верифікується на лабораторному стенді із супровідними розрахунками параметрів якості сигналу. Стендові вимірювання доповнюються програмним моделюванням. Головний пристрій PLC отримує дані для передавання з NFC-V EEPROM, обробляє їх та формує відповідну аналогову форму сигналу для інжекції. У статті наведено детальний аналіз і опис протоколу NFC-V, разом із прикладами осцилограм захоплення та декодування комунікаційного сигналу. У результаті обробки сигналу головний контролер PLC формує аналоговий сигнал певної послідовності, який інжектується у зворотний зв'язок імпульсного перетворювача. Цей сигнал розглядається як фізичний рівень спеціального типу для запропонованого протоколу зв'язку. Вузол, підключений до силової лінії, живиться від передавача. Вузол використовує лише позитивний та негативний термінали живлення як канали для одночасного передавання даних і потужності. Отриманий модульований сигнал проходить через смуговий фільтр із центральною частотою 15 кГц, смугою пропускання 158 МГц і підсиленням 20 дБ. Операції аналого-цифрового декодування виконує спеціалізована гібридна мікросхема (ASIC). Результати декодування перевіряються на лабораторному стенді із візуалізацією процесу перетворення сигналу з ASK у SPI. Модульований сигнал, інжектований у силову лінію, порівнюється з сигналом, що повертається зі смугового фільтра PLC-вузла після етапів зрізу частот та підсилення. У статті наведено аналіз показників якості сигналу та зроблено висновки щодо ефективності запропонованої системи.

Ключові слова: *імпульсний перетворювач, зворотний зв'язок, модуляція, THD, SNR, NFC.*